TS81102G0FS
DMUX 8/10-bit 1:4/1:8 1.5 Gsps

Datasheet

Main Features

- Programmable DMUX Ratio:
  - 1:4 Data Rate Max = 750 Msps
  - P_D (8b/10b) < 4.3/4.7W (ECL 50Ω Output)
  - 1:8 Data Rate Max = 1.5 Gsps
  - P_D (8b/10b) < 6/6.9W (ECL 50Ω Output)
  - 1:16 with 1 TS8388B or 1 TS83102G0 and 2 DMUX
- Parallel Output Mode
- 8/10-bit
- ECL Differential Input Data
- Data Ready or Data Ready/2 Input Clock
- Input Clock Sampling Delay Adjust
- Single-ended Output Data:
  - Adjustable Common Mode and Swing
  - Logic Threshold Reference Output
  - ECL, PECL, TTL
- Asynchronous Reset
- Synchronous Reset
- ADC and DMUX Multi-channel Applications:
  - Stand-alone Delay Adjust Cell for ADCs Sampling Instant Alignment
- Differential Data Ready Output
- Built-in Self Test (BIST)
- Dual Power Supply V_{EE} = -5V, V_{CC} = 5V
- Radiation Tolerance Oriented Design (More Than 100 Krad (Si) Expected)
- Thermally Enhanced CQFP196 Cavity Up Package

Screening

- Temperature Range:
  - C Grade: 0°C < T_C; T_J < 90°C
  - V Grade: -40°C < T_C-; T_J< 110°C
  - M Grade: -55°C < T_C; T_J< 125°C
- Standard Screening Level for “C”, “V” and “M” Grades
- ESA SCC 9000 Space Screening Flow for “M” Grade (on Request)

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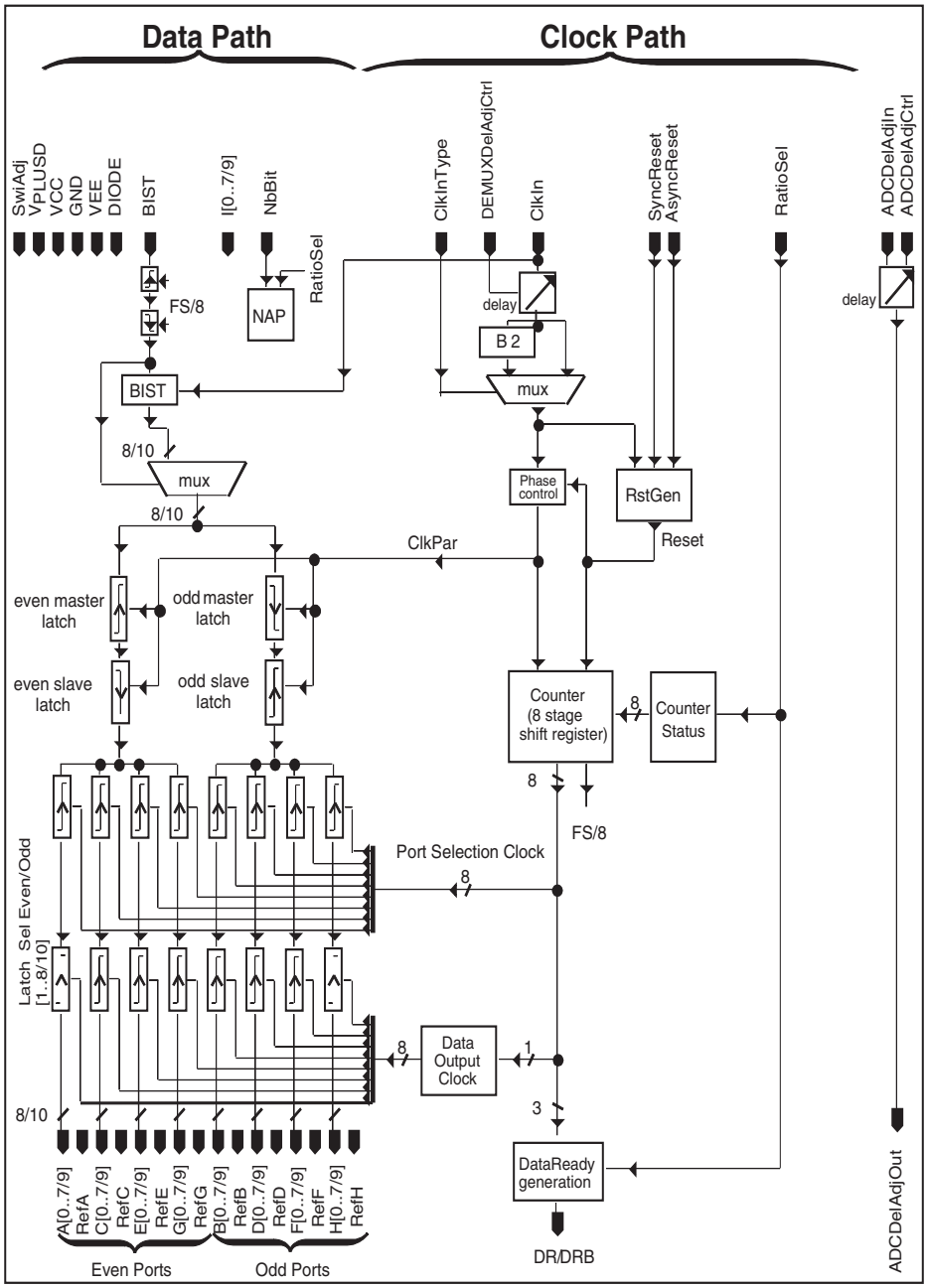
1. Description

The TS81102G0 is a monolithic 10-bit high-speed (up to 1.5 Gsps) demultiplexer. The DMUX is designed to run with all kinds of ADCs and more specifically, it fits perfectly with e2v high speed ADC 8-bit 1 Gsps TS8388B, ADC 10-bit 2 Gsps TS83102G0B.

The TS81102G0 is using a well proven architecture, including a delay control and tunable output levels.

This DMUX allows users to process the high speed output data stream down to standard signal processors speed (standard FPGAs).

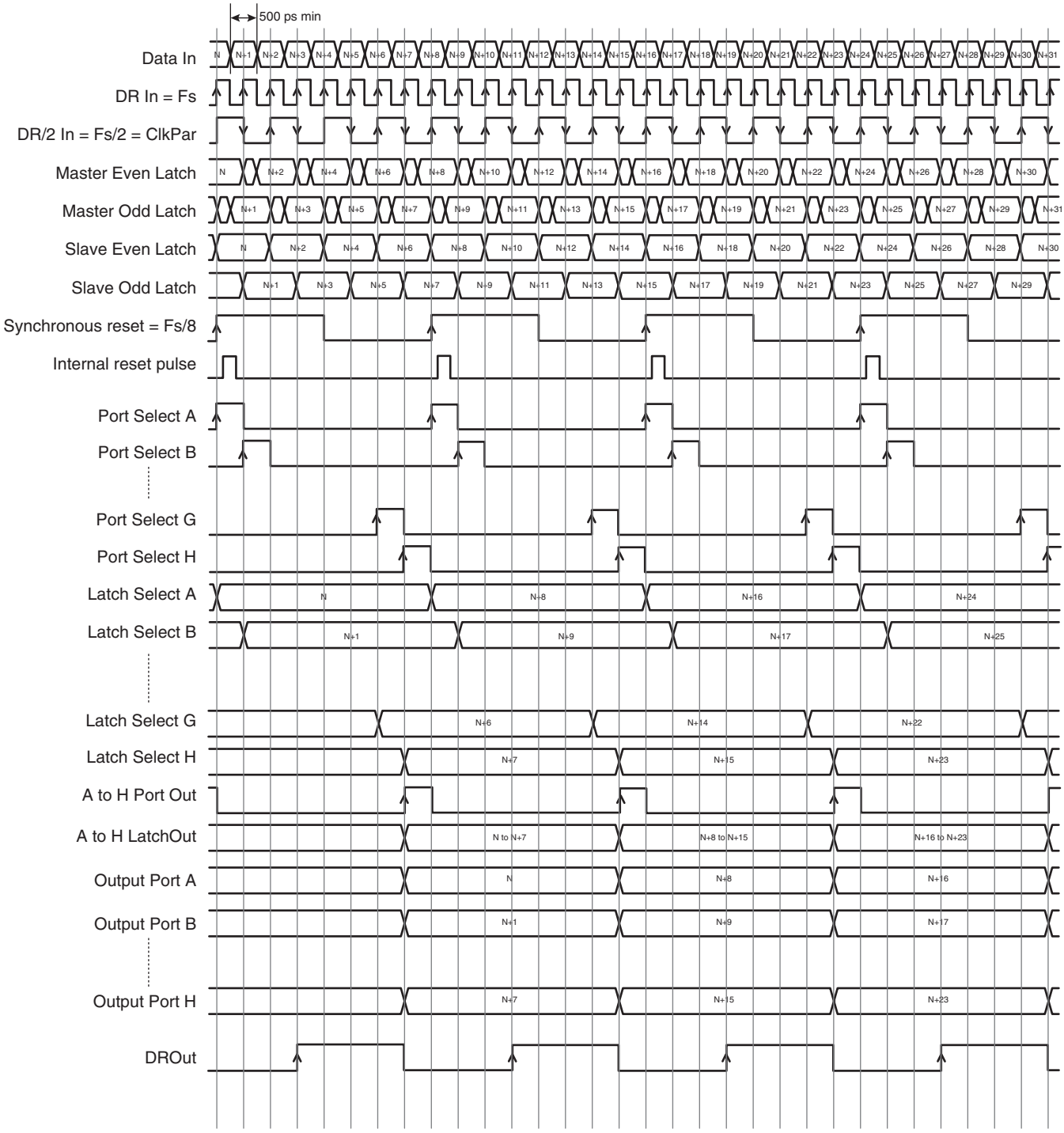
2. Block Diagram



3. Internal Timing Diagram

This diagram is corresponding to an established operation of the DMUX with Synchronous Reset.

Figure 3-1. Timing Diagram



4. Functional Description

Its role is to reduce the data rate so that the data could be processed at the DEMUX output.The TS81102G0 provides 2 programmable ratios: 1:4 and 1:8.The maximum input data rate is 750 Msps for 1:4 ratio and 1.5 GSPS for 1:8 ratio. The TS81102G0 is able to process 8 or 10 bits data flow. The input clock can be ECL differential signal or single-ended DC coupled signal. Moreover the user can choose between a Data Ready "DR mode" (the rising edge of the clock corresponds to a valid data) or Data Ready/2 "DR/2 mode" (each edge of the clock corresponds to a valid data) clock.

The input digital data must be ECL differential signals. The output signals (Data Ready, digital data and reference voltage) are adjustable with V_{PLUSD} independent power supply. Typical output modes are ECL, PECL or TTL. The Data Ready output is a differential signal. The digital output data are pseudo single-ended signals since a Reference voltage giving the common mode of the output data is provided for each port.

The TS81102G0 is started by an Asynchronous Reset. This reset acts as a master reset for the DMUX. A Synchronous Reset enables to re-synchronize the output port selection at each new data cycle and to minimize possible loss of data that could occur within the DMUX (in case of Single Event Upset possibilities).

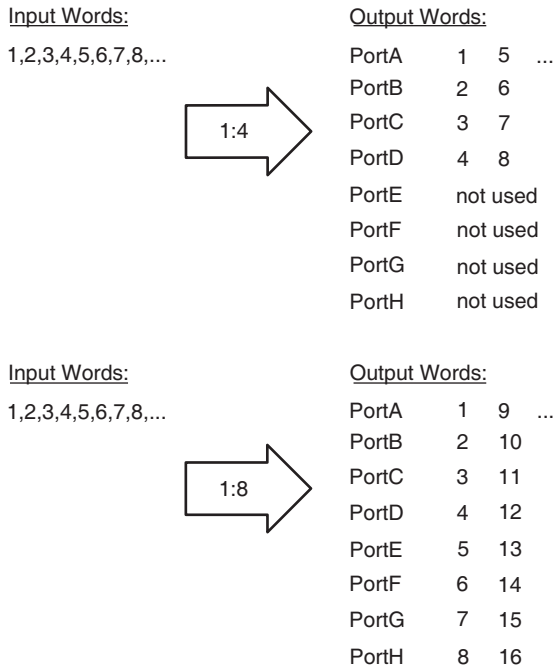
A delay adjust cell is available to ensure a good phase between input clock and input data of the DEMUX (DMUXDelAdjCtrl function). Another delay adjust cell is available to control ADCs sampling instant alignment, in case of ADCs interleaving. This is a stand-alone delay cell (ADCDelAdjCtrl Function). A 10 bits generator is implemented in the TS81102G0, the Built-In Self Test (BIST). This test sequence is very useful for testing the DMUX at first use. A fine tuning of the output swing is also available (SwiAdj). The TS81102G0 can be used with all e2v-Grenoble ADCs.

5. Main Functions Description

5.1 Programmable DMUX Ratio

The conversion ratio is programmable: 1:4 or 1:8.

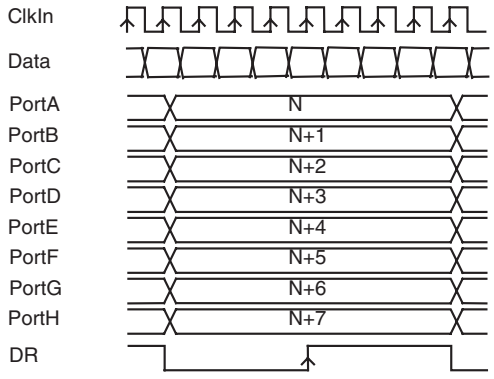
Figure 5-1. Programmable DMUX Ratio



Note: When the DMUX is used in 1:4 ratio, the unused ports can be left floating.

5.2 Parallel Output Mode

Figure 5-2. Parallel Mode

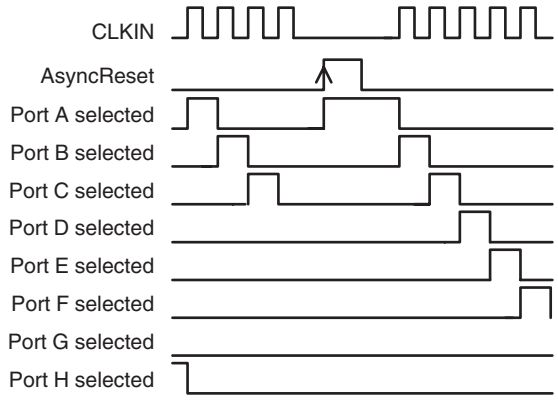


5.3 Input Clock Sampling Delay Adjust (DEMUXDELADJCTRL)

The input clock phase can be adjusted with an adjustable delay (from 250 ps to 750 ps). This is to ensure a good phase between clock and input data of the DMUX.

5.4 Asynchronous Reset (ASYNCRESET)

Figure 5-3. Asynchronous Reset

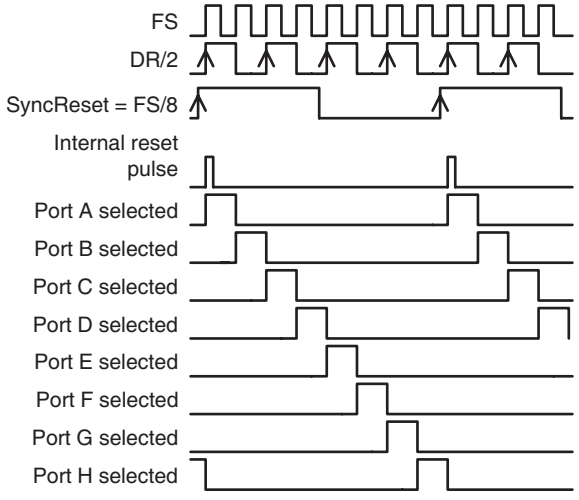


The Asynchronous Reset is a master reset of the port selection, which works on TTL levels. It is active on the high level. During an asynchronous reset, the clock must be in a known state. It is used to start the DMUX.

When it is active, it is paralyzing the outputs (output clock and output data remain to the level they had, just before the asynchronous reset). When it comes back to its low level, the DMUX starts: the outputs are active and the first processed data is on the port A.

5.5 Synchronous Reset (SYNCRESET)

Figure 5-4. Synchronous Reset



The DMUX can be synchronously reset to a programmable state depending on the conversion ratio. The clock must not be stopped during synchronous reset. The synchronization signal is a clock (SyncRest) which frequency is like FS/8*n in 1:8 mode (where FS is the input clock frequency and n is an integer (n=1,2,3,…)) and FS/4*n in 1:4 mode. The front edge of this clock is synchronized with ClkIn inside the DMUX, and generates a 200ps reset pulse. This reset pulse occurs during a fixed level of ClkIn.

If the DMUX was synchronized with Syncreset previous to the synchronous reset, then the output data are immediately correct, no modification can be seen at the output of the DMUX, and no data are lost (see “Internal Timing Diagram” on page 3).

If the DMUX was not synchronized with SyncReset, then the output data and data ready of the DMUX are changed. The output data are correct after a number of input clock corresponding to the pipeline delay (see examples page 19).

5.6 Pipeline Delay

The maximum pipeline delay depends on the conversion ratio:

- 1:8: pipeline delay = 7 clock cycles
- 1:4: pipeline delay = 3 clock cycles

5.7 8/10-bit, with NAP Mode for the 2 Unused bit

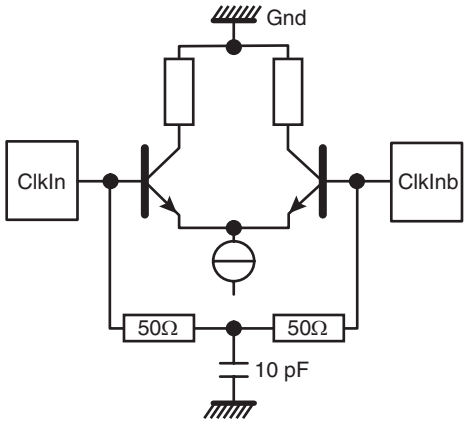
The DMUX is a 10-bit parallel device. The two last bit (bit 8 and 9) may not be used, and the corresponding functions are set in nap mode to reduce power consumption.

5.8 ECL Differential Input Data

Input data are ECL compatible (Voh = - 1.1V, Vol = - 1.6V). The minimum swing required is 100 mV differential.

All inputs have a 100Ω differential termination resistor. The middle point of these resistors is connected to ground through a 10 pF capacitor:

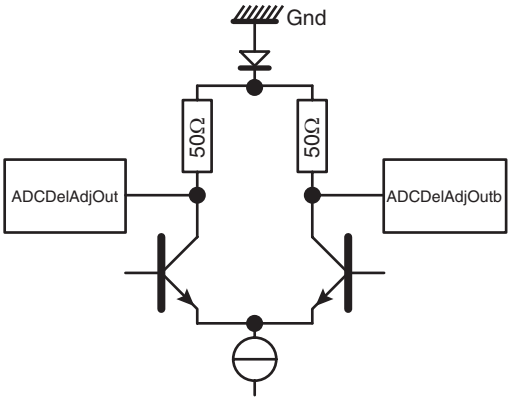
Figure 5-5. ECL Differential Input Data



5.9 50Ω Differential Output Data

The differential ADCDelAdjOut/ADCDelAdjOutb signal is generated through 50Ω loaded long tailed. The 50Ω resistor is connected to ground pad through a diode. The levels are (on 100Ω differential termination resistor): Vol = - 1.9V, Voh = - 1.1V.

Figure 5-6. 50Ω Differential Output Data

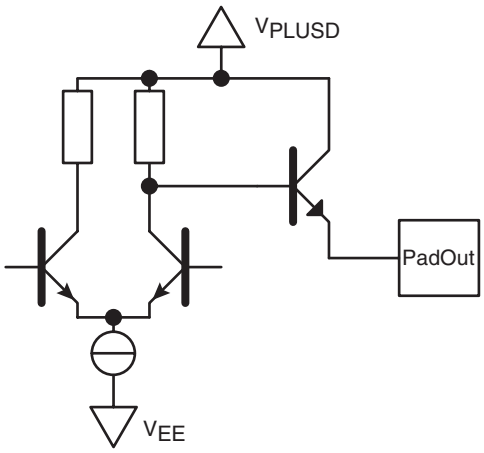


5.10 Single-ended Output Data

To reduce the pin number of the DMUX, and the power consumption, the eight output ports are single ended. To reach the high frequency output (up to 93.75 MHz, that is 187.5 Msps rate), with a reasonable power consumption, the swing must be limited to a maximum of ± 500 mV. The common mode is adjustable from -1.3V to + 2V, with V_{PLUSD} pins.

To ensure a better noise immunity, a reference level (common mode) is available (one by output port). The output buffers are ECL type (open emitter - not a resistive adapted impedance). They are designed for 15 mA average output current, and may be used with a 50Ω termination impedance.

Figure 5-7. Single-ended Output Data



We give thereafter three examples of application of these buffers: ECL/PECL/TTL. Please note that it is possible to have any other odd output format as far as current (36 mA max) and voltage (V_{PLUSD} - $V_{EE} \leq$ 8.3V) limits are not overridden. The maximum frequency in TTL output mode depends on the load to drive (see "Switching Performance and Characteristics" on page 13).

Table 5-1. Theoretical Output Levels

Parameter	ECL	PECL	TTL
V_{PLUSD}	0V	3.3V	3.3V
Vtt	-2V	1.3V	0V
Swing	±0.5V	±0.5V	±1V
Reference	-1.6V	1.7V	1.6V
Voh	-1.1V	2.3V	2.5V
Vol	-1.9V	1.3V	0.5V
Load	50Ω	50Ω	≥ 75Ω
Average Output Current	14 mA	14 mA	15 mA
Max Output Data Rate	187.5 MSPS	187.5 MSPS	187.5 MSPS

Note: The max Output data rate is given for a typical 50Ω //2 pF load in ECL and PECL and 75Ω //2 pF load in TTL.

5.11 Differential Data Ready Output:

The front edge of the Data Ready Output occurs when data is available on the corresponding port. The frequency of this clock depends on the conversion ratio (1:8 or 1:4), with a duty cycle of 50%.

The levels of this signal are the same as the output data: Nevertheless, the Data Ready output buffer is differential.

5.12 Built-in Self Test (BIST)

A pseudo-random 10 bit generator is implemented in the DMUX. It generates a 10 bit signal in the output of the DMUX, with a period of 512 input clock. The probability of occurrence of codes is uniformly spread over the 1024 possible codes: 0 or 1/1024.

Note that the 256 codes of bit 1 to 8 occur at least once. It starts with Bist command, in phase with FS/8 clock, on Port A. The logic output obtained on the A to H ports depends on the conversion ratio. The driving clock of BIST is ClkIn. The ClkInType must be set to *1* (Data Ready ADC clock) to have a different 10 bit code on each output. If ClkInType is set to *0* (DR/2 mode), then the same code repeats on two consecutive ports: N on port A, N on port B, N+1 on port C, N+1 on port D, etc.

The complete BIST sequence is available on request.

6. Specifications

6.1 Absolute Maximum Ratings

Table 6-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Positive output buffer supply voltage	V_{PLUSD}		GND to 4	V
Negative supply voltage	V_{EE}		GND to -6	V
Analog input voltages	ADCDelAdjCtrl; ADCDelAdjCtrlb DMUXDelAdjCtrl; DMUXDelAdjCtrlb SwiAdj	Voltage range for each pad Differential voltage range	-1 to +1 -1 to +1	V
ECL 50Ω input voltage	ClkIn; ClkInb I[0…9]; I[0…9]b SyncReset; SyncResetb ADCDelAdjIn; ADCDelAdjInb	Voltage range for each pad	-2.2 to +0.6	V
Maximum difference between ECL 50Ω input voltages	ClkIn; ClkInb I[0…9]; I[0…9]b SyncReset; Syncresetb ADCDelAdjIn; ADCDelAdjInb	Minimum differential swing Maximum differential swing	0.1 2	V
Data output current	A[0…9] to H[0…9] RefA to RefH DR; DRb	Maximum current	36	mA
TTL input voltage	ClkIn Type RatioSel NbBit AsyncReset BIST		GND to V_{CC}	V
Maximum input voltage on diode for temperature measurement	DIODE		700	mV
Maximum input current on diode	DIODE		8	mA
Maximum junction temperature	T_J		135	°C
Storage temperature	T_{stg}		-65 to 150	°C

Note: Absolute maximum ratings are limiting values, to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. *The use of a thermal heat sink is mandatory.*

6.2 Recommended Conditions of Use

Table 6-2. Recommended Operating Conditions

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Positive supply voltage	V_{CC}		–	5	–	V
Positive output buffer supply voltage	V_{PLUSD}	ECL output compatibility	–	0	–	V
	V_{PLUSD}	PECL output compatibility	–	3.3	–	V
	V_{PLUSD}	TTL output compatibility	–	3.3	–	V
Negative supply voltage	V_{EE}		–	-5	–	V
Operating temperature range	T_J	Commercial grade: “C” Industrial grade: “V” Military grade: “M“	“C” grade: $0 < T_C$; $T_J < +90$ “V” grade: $-40 < T_C$; Tc- $< +110$ “M” grade: $-55 < T_C < +125$			°C

6.3 Electrical Operating Characteristics

T_J (typical) = 70°C. full temperature range: $-55°C < T_C$; $T_J < +125°C$.

Table 6-3. Electrical Specifications

Parameter	Symbol	Test Level	Value			Unit
			Min	Typ	Max	
Positive supply voltage V_{CC}	V_{CC}	1	4.75	5	5.25	V
V_{PLUSD}						
ECL	V_{PLUSD}		-0.25	0	0.25	
PECL	V_{PLUSD}		3.135	3.3	3.465	
Positive supply voltage V_{PLUSD}						
TTL	V_{PLUSD}	4	3.135	3.3	3.465	V
Negative supply voltage V_{EE}	V_{EE}	1	-5.25	-5	-4.75	V
Supply Currents						
ECL (50Ω) and PECL (50Ω) V_{CC} (for every configuration)						
	I_{CC}		–	31	50	
1:8, 8 bits	I_{PLUSD}		540	1180	1820	
	I_{EE}		–	720	800	
1:8, 10 bits	I_{PLUSD}	1	640	1140	2240	
	I_{EE}		–	790	850	mA
1:4, 8 bits	I_{PLUSD}		270	590	910	
	I_{EE}		–	590	650	
1:4, 10 bits	I_{PLUSD}		320	720	1120	
	I_{EE}		–	640	700	

Table 6-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit
			Min	Typ	Max	
TTL (75Ω)						
V_{CC} (for every configuration)						
	I_{CC}		–	30	50	
1:8, 8 bits	I_{PLUSD}		760	1610	2440	
	I_{EE}		–	870	930	
1:8, 10 bits	I_{PLUSD}	4	900	1770	3010	mA
	I_{EE}		–	980	1060	
1:4, 8 bits	I_{PLUSD}		380	810	1220	
	I_{EE}		–	670	730	
1:4, 10 bits	I_{PLUSD}		450	880	1510	
	I_{EE}		–	730	800	
Nominal power dissipation						
ECL (50Ω)						
1:8, 8 bits	PD	1	5.2	5.6	6.0	W
1:8, 10 bits	PD		5.9	6.4	6.9	W
1:4, 8 bits	PD		3.9	4.1	4.3	W
1:4, 10 bits	PD		4.2	4.5	4.7	W
PECL (50Ω)						
1:8, 8 bits	PD	1	5.8	6.2	6.6	W
1:8, 10 bits	PD		6.6	7.1	7.6	W
1:4, 8 bits	PD		4.2	4.4	4.6	W
1:4, 10 bits	PD		4.6	4.8	5.1	W
TTL (75Ω)						
1:8, 8 bits	PD	4	6.8	7.3	7.7	W
1:8, 10 bits	PD		7.8	8.4	9	W
1:4, 8 bits	PD		4.7	4.9	5.1	W
1:4, 10 bits	PD		5.2	5.5	5.8	W
Delay Adjust Control						
DMUXDelAdjCtrl differential voltage	DDAC					
250 ps		5	–	-0.5	–	V
500 ps			–	0	–	V
750 ps			–	0.5	–	V
Input current	IDDAC		–	20	–	µA
ADCDelAdjCtrl differential voltage	ADAC					
250 ps		5	–	-0.5	–	V
500 ps			–	0	–	V
750 ps			–	0.5	–	V
Input current	IADAC		–	20	–	µA

Table 6-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit
			Min	Typ	Max	
Digital Outputs						
ECL Output (assuming V_{PLUSD} = 0V, SWIADJ = 0V, 50Ω termination resistor on board)						
Logic “0” voltage	V_{OL}	1		-1.90	-1.80	V
Logic “1” voltage	V_{OH}		-1.50	-1.10		V
Reference voltage	V_{REF}		-1.90	-1.60	-1.30	V
PECL Output (assuming V_{PLUSD} = 3.3V, SWIADJ = 0V, 50Ω termination resistor on board)						
Logic “0” voltage	V_{OL}	4		1.30	1.45	V
Logic “1” voltage	V_{OH}	4	2.00	2.30		V
Reference voltage	V_{REF}	4	1.40	1.70	2.00	V
TTL Output (assuming V_{PLUSD} = 3.3V, SWIADJ = 0V, 75Ω termination resistor on board)		4				
Logic “0” voltage	V_{OL}			1.00	1.20	V
Logic “1” voltage	V_{OH}		1.95	2.20		V
Reference voltage	V_{REF}		1.30	1.60	1.90	V
Output level drift with temperature (data and DR outputs)		4		-1.3		mV/°C
Output level drift with temperature (reference outputs)				-0.9		mV/°C
Digital Inputs						
DATA Input Voltages (ECL)						
Logic “0” voltage	V_{IL}	1			-1.6	V
Logic “1” voltage	V_{IH}		-1.1			V
CTRL Input Voltages (TTL)						
Logic “0” voltage	V_{IL}	1			0.6	V
Logic “1” voltage	V_{IH}		2.0			V

Note:
1. The supply current IPLUSD and the power dissipation depend on the state of the output buffers
2. The minimum values correspond to all the output buffers at low level
3. The maximum values correspond to all the output buffers at high level
4. The typical values correspond to an equal sharing-out of the output buffers between high and low levels

6.4 Switching Performance and Characteristics

- 50% clock duty cycle (CLKIN, CLKINB). T_J (typical) = 70°C.
- Full temperature range: -55°C < T_C; T_J < +125°C.
- See Timing Diagrams Figure 6-1 on page 17 to Figure 6-8 on page 21.

Table 6-4. Switching Performances

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	Typ	Max		
Input Clock							
Maximum clock frequency 1:8 ratio DR input clock DR/2 input clock 1:4 ratio DR input clock DR/2 input clock	FMAX	4	 1500 750 750 375			MHz	
Maximum output data rate	FDATAMAX	4	187.5			Msps	
Clock pulse width (high)	TC1	4	225	–	–	ps	
Clock pulse width (low)	TC2	4	225	–	–	ps	
Clock Path pipeline delay DR input clock DR/2 input clock	 TCPD TCPD	4	 – –	 980 1090	 – –	 ps ps	 (1) (2)
Clock rise/fall time	TRCKIN TFCKIN	4	–	100	–	ps	
Asynchronous Reset							
Asynchronous Reset pulse width	PWAR	4	2000	–	–	ps	
Setup time from Asynchronous to Clkln	TSAR	4	–	200	–	ps	
Synchronous Reset							
Setup time from SyncReset to Clkln DR input clock DR/2 input clock	TSSR	4	 – –	 -580 -480	 – –	 ps ps	 (3) (4)
Hold time from Clkln to SyncReset DR input clock DR/2 input clock	THSR	4	 – –	 780 680	 – –	 ps ps	 (5) (6)
Rise/fall for (10% to 90%)	TSRR/TFSR	4	100	–	–	ps	
Input Data							
Setup time from I[0…9] to Clkln DR input clock DR/2 input clock	TSCKIN	4	 – –	 -800 -690	 – –	 ps ps	 (7) (8)
Hold time from Clkln to I[0…9] DR input clock DR/2 input clock	THCKIN	4	 – –	 1000 890	 – –	 ps ps	 (9) (10)
Rise/fall for (10% to 90%)	TRDI/TFDI	4	100	–	–	ps	

Table 6-4. Switching Performances (Continued)

Parameter	Symbol	Test Level	Value Min	Value Typ	Value Max	Unit	Note
Output Data							
Data output delay DR input clock DR/2 input clock	TOD	4	– –	1820 1720	– –	ps ps	(11) (12)
Data pipeline delay DR input clock, 1:4 ratio DR input clock, 1:8 ratio DR/2 input clock, 1:4 ratio DR/2 input clock, 1:8 ratio	TPD	4	 – – – –	 3 7 3/2 7/2	 – – – –	Number of input clock	(13)
Rise/fall for (10% – 90%)	TROD/TFOD	4	–	500/500	–	ps	(14)
Data Ready							
Clock to Data Ready falling edge DR input clock DR/2 input clock	TDRF	4	 – –	 3080 2500	 – –	 ps ps	 (15) (16)
Clock to Data Ready rising edge DR input clock DR/2 input clock	TDRR	4	 – –	 3180 2750	 – –	 ps ps	 (17) (18)
Asynchronous Reset to DataReady delay	TARDR	4	–	2820	–	ps	(19)
Synchronous Reset to DataReady delay	TSRDR	4	–	1500	–	ps	(20)
Rise/fall for (10% – 90%)	TRDR/TFDR	4	–	380/260	–	ps	(21)
Rising edge uncertainty	JITTER	4	–	20	–	ps rms	
Setup time from Bist to ClkIn	TSBIST	4	–	1000	–	ps	
Rise/fall time for (10% – 90%)	TRBIST/ TFBIST	4	1000	–	–	ps	
ADC Delay Adjust							
Input frequency	FMADA	4	1.5	–		GHz	
Input pulse width (high)	TC1ADA	4	180	–	–	ps	
Input pulse width (low)	TC2ADA	4	180	–	–	ps	
Input rise/fall time	TRIADA/ TFIADA	4	70 60	150 150	– –	ps	
Output rise/fall time	TROADA/ TFOADA	4	– –	150 100	– –	ps	(22)
Data output delay (typical delay adjust setting)	TADA	4	– –	800 900	– –	ps	(23) (24)
Output delay drift with temperature	TADAT	4	–	2.5	–	ps/°C	
Output delay uncertainly	JITADA	4	–	20	–	ps rms	

Note: 1. TCPD is tuned with DMUXDelAdjCtrl: TCPD = 980 ± 250 ps.
2. TCPD is tuned with DMUXDelAdjCtrl: TCPD = 1090 ± 250 ps.

3. TSSR depends on DMUXDelAdjCtrl: TSSR = -580 ± 250 ps. TSSR < 0 because of Clock Path internal delay.
4. TSSR depends on DMUXDelAdjCtrl: TSSR = -480 ± 250 ps. TSSR < 0 because of Clock Path internal delay.
5. THSR depends on DMUXDelAdjCtrl: THSR = 780 ± 250 ps.
6. THSR depends on DMUXDelAdjCtrl: THSR = 680 ± 250 ps.
7. TSCKIN depends on DMUXDelAdjCtrl: TSCKIN = -800 ± 250 ps. TSCKIN < 0 because of Clock Path internal delay.
8. TSCKIN depends on DMUXDelAdjCtrl: TSCKIN = -690 ± 250 ps. TSCKIN < 0 because of Clock Path internal delay.
9. THCKIN depends on DMUXDelAdjCtrl: THCKIN = 1000 ± 250 ps.
10. THCKIN depends on DMUXDelAdjCtrl: THCKIN = 890 ± 250 ps.
11. TOD depends on DMUXDelAdjCtrl: TOD = 1820 ± 250 ps. TOD is given for ECL 50Ω/2 pFoutput load.
12. TOD depends on DMUXDelAdjCtrl: TOD = 1720 ± 250 ps. TOD is given for ECL 50Ω/2 pFoutput load.
13. TPD is the number of ClkIn clock cycle from selection of Port A to selection of Port H in 1:8 conversion mode, and from selection of Port A to selection of Port D in 1:4 conversion mode. It is the maximum number of ClkIn clock cycle, or pipeline delay, that a data has to stay in the DMUX before being sorted out. This maximum delay occurs for the data sent to Port A. For instance, the data sent to Port H goes directly from the input to the Port H, and its pipeline is 0. But even for this data, there is an additional delay due to physical propagation time in the DMUX.
14. TROD and TFOD are given for ECL 50Ω/2 pF output load. In TTL mode, the TROD and TFOD are twice the ones for ECL. (For other termination topology, apply proper derating value 50 ps/pF in ECL, 100 ps/pF in TTL mode.)
15. TDRF depends on DMUXDelAdjCtrl: TDRF = 3080 ± 250 ps. It is given for ECL 50Ω/2 pF output load.
16. TDRF depends on DMUXDelAdjCtrl: TDRF = 2500 ± 250 ps. It is given for ECL 50Ω/2 pF output load.
17. TDRR depends on DMUXDelAdjCtrl: TDRR = 3180 ± 250 ps. It is given for ECL 50Ω/2 pF output load.
18. TDRR depends on DMUXDelAdjCtrl: TDRR = 2750 ± 250 ps. It is given for ECL 50Ω/2 pF output load.
19. TARDR is given for ECL 50Ω/2 pF output load.
20. TSRDR is given for ECL 50Ω/2 pF output load. It is minimum value since RstSync clock is synchronized with ClkIn clock.
21. TRDR and TFDR are given for ECL 50Ω/2 pF output load.
22. With transmission line (ZO = 50Ω) and output load R = 50Ω; C = 2 pF.
23. Without output load.
24. With transmission line (ZO = 50Ω) and output load R = 50Ω; C = 2 pF.

6.4.1 Explanation of Test Levels

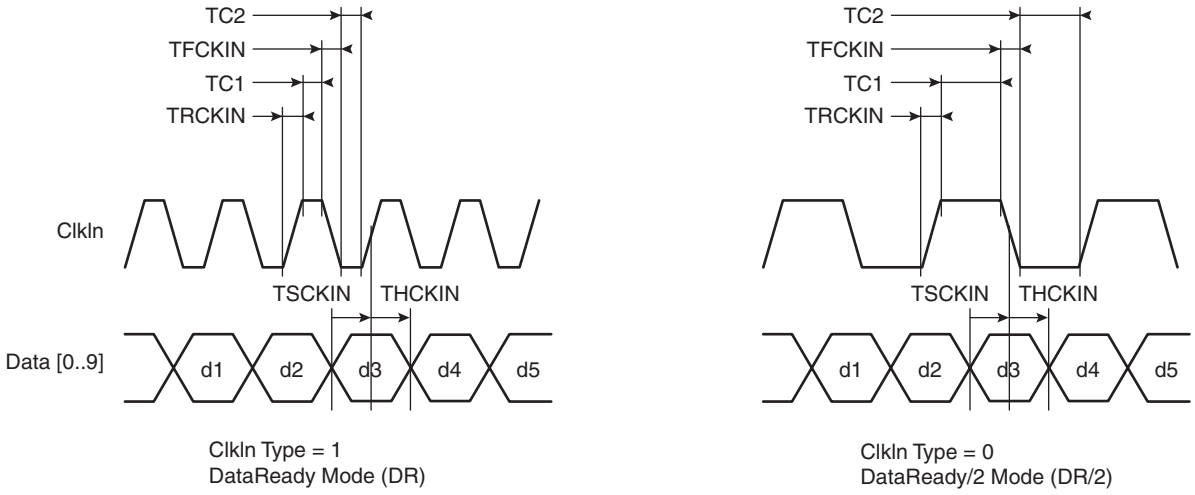
Table 6-5. Explanation of Test Levels

Num	Characteristics
1	100% production tested at + 25°C or three temperature (min, ambient, max) for ESA/SCC screening flow
2	100% production tested at + 25°C , and sample tested at specified temperature
3	Sample tested only at specified temperature
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature)
5	Parameter is a typical value only

Notes: 1. Only Min and Max values are guaranteed (typical values are issuing from characterization results).
2. The level 1 and 2 tests are performed at 50 MHz.

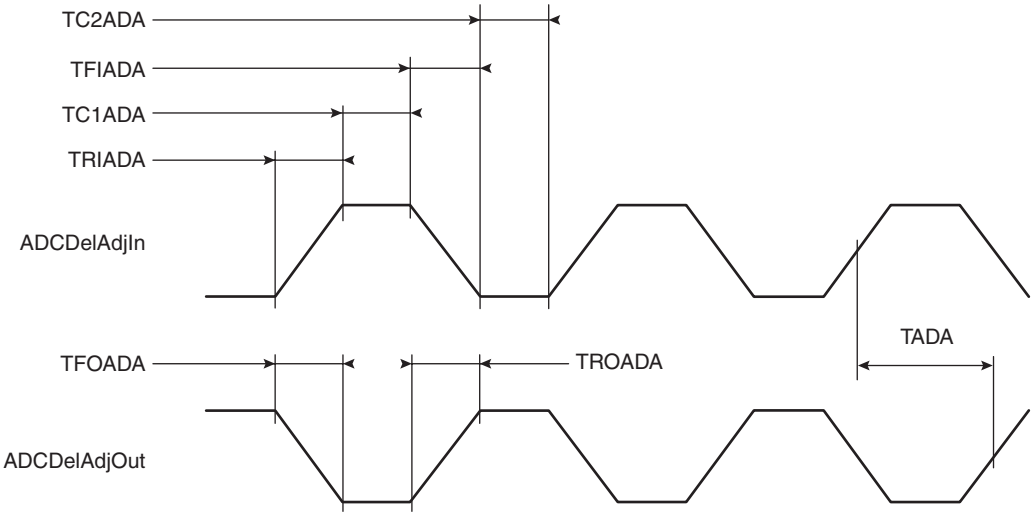
6.4.2 Input Clock Timings

Figure 6-1. Input Clock



6.4.3 ADC Delay Adjust Timing Diagram

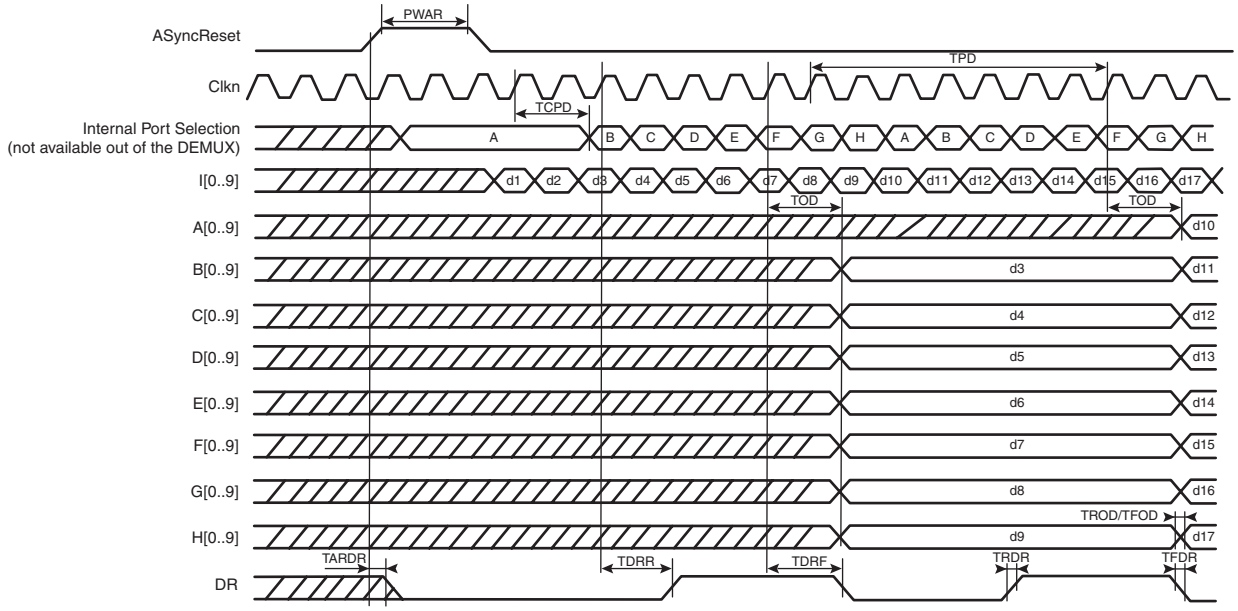
Figure 6-2. ADC Delay Adjust Timing Diagram



6.4.4 Timing Diagrams with Asynchronous Reset

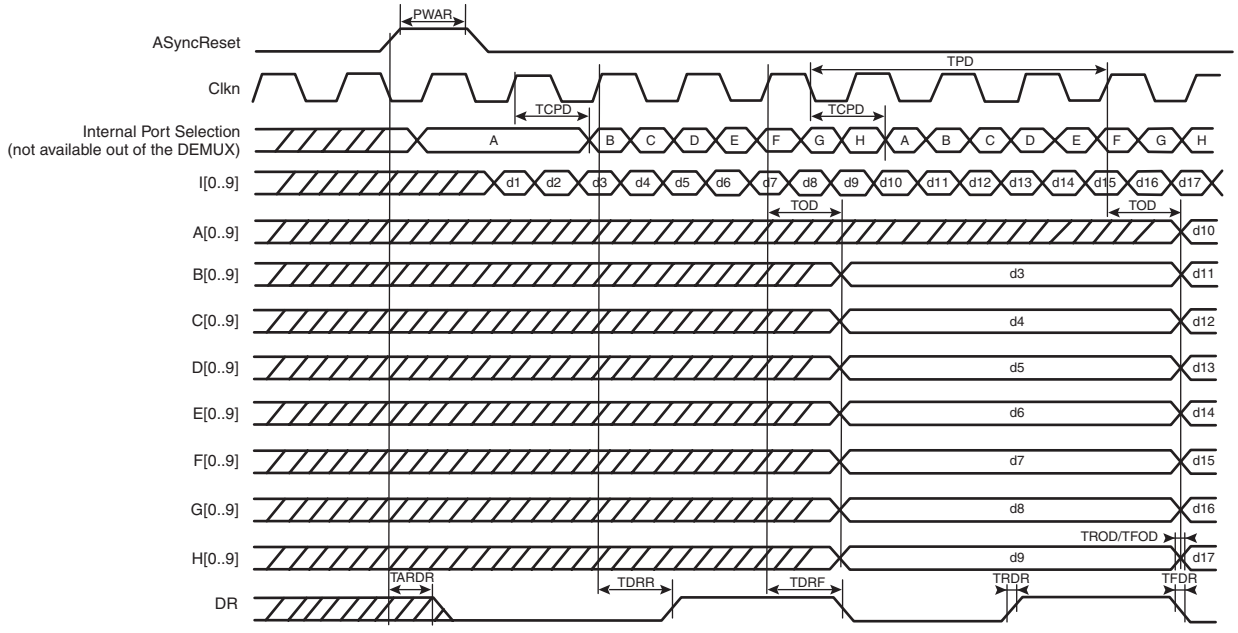
With a nominal tuning of DMUXDelAdjCtrl at a frequency of 1.5 GHz, d1 and d2 data are lost because of internal clock path propagation delay TCPD. TCPD is tuned with DMUXDelAdjCtrl pins to have good setup and hold times between ClkIn and Data.

Figure 6-3. Start with Asynchronous Rest, 1:8 Ratio, DR Mode



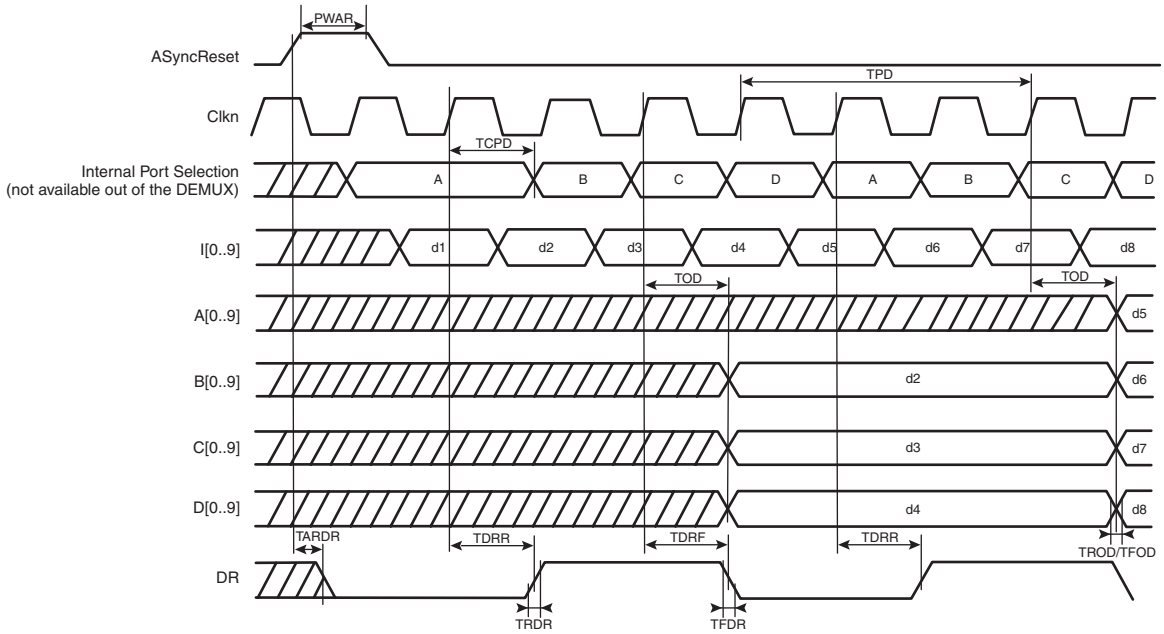
With a nominal tuning of DMUXDelAdj at 1.5 GHz, d1 and d2 data are lost because of internal clock path propagation delay TCPD. TCPD is tuned with DMUXDelAdjCtrl pins to have good setup and hold times between ClkIn and input data. This timing diagram does not change with the opposite phase of ClkIn.

Figure 6-4. Start with Asynchronous Rest, 1:8 Ratio, DR/2 Mode



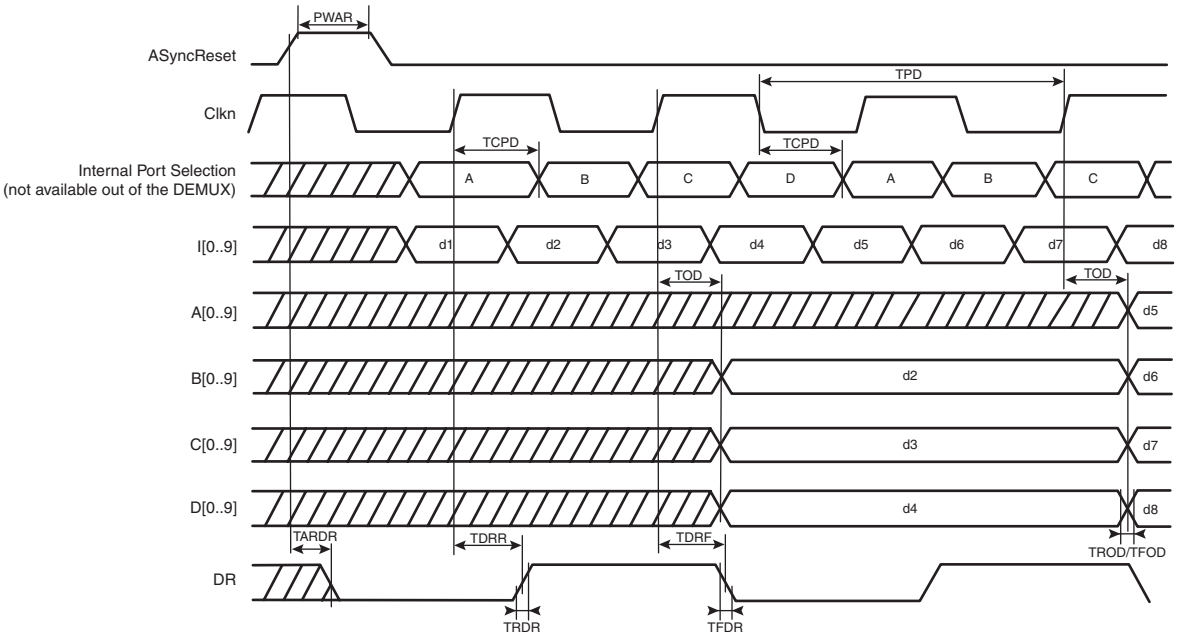
With a nominal tuning of DMUXDelAdj, at 750 MHz (1:4 mode) d1 data is lost because of internal clock path propagation delay TCPD. TCPD is tuned with DMUXDelAdjCtrl pins and is used to have good setup and hold times between ClkIn and input data.

Figure 6-5. Start with Asynchronous Reset, 1:4 Ratio, DR Mode



With a nominal tuning of DMUXDelAdj, at 750 MHz (1:4 mode) d1 data is lost because of internal clock path propagation delay TCPD. TCPD is tuned with DMUXDelAdjCtrl pins and is used to have good setup and hold times between ClkIn and input data. This timing diagram does not change with the opposite phase of ClkIn.

Figure 6-6. Start with Asynchronous Reset, 1:4 Ratio, DR/2 Mode



6.4.5 Timing Diagrams with Synchronous Reset

Examples of Synchronous Reset usefulness in case of desynchronization of DMUX output port selection.

6.4.5.1 Synchronous Reset, 1:8 Ratio, DR Mode

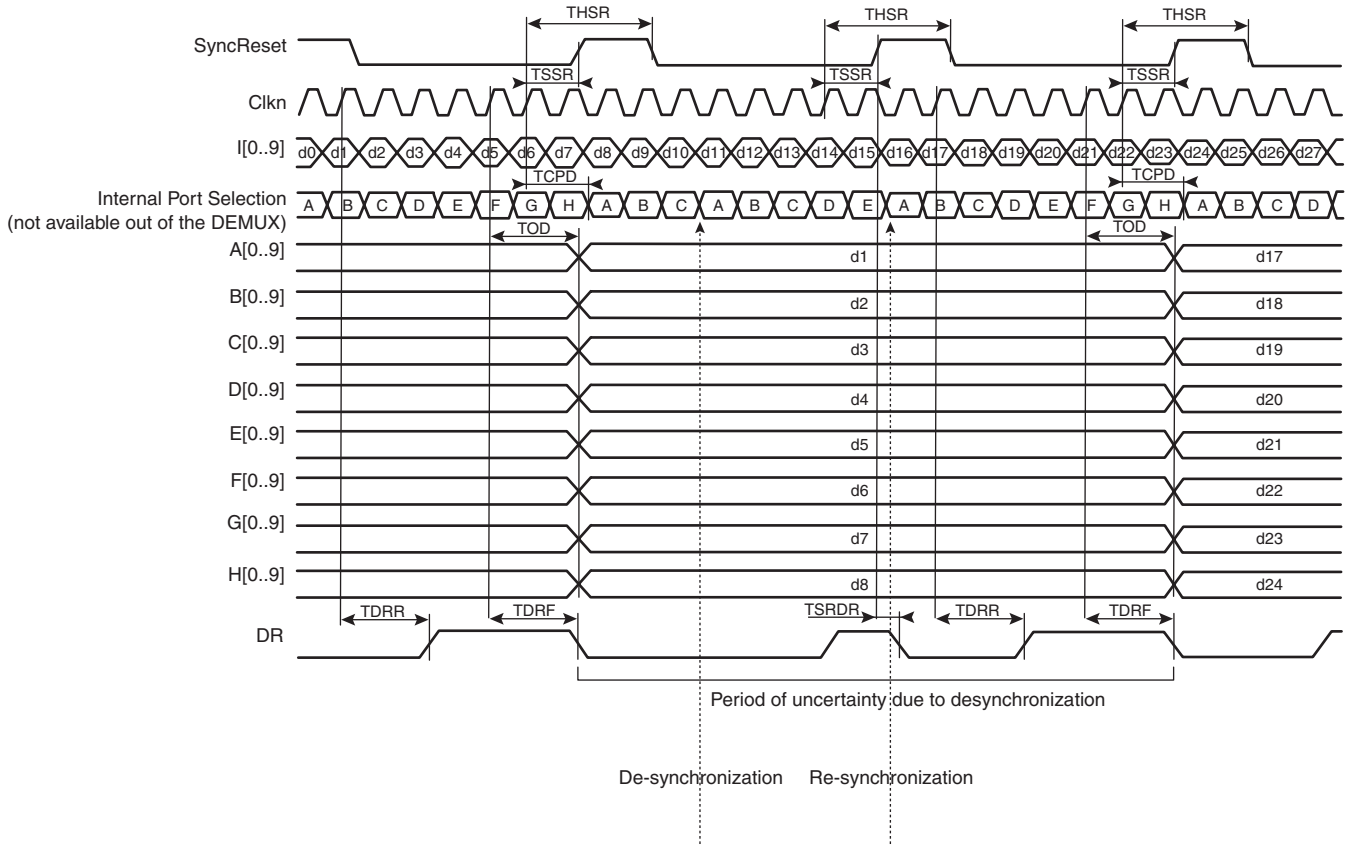
The desynchronization event happens after the selection of Port C.

DMUXDelAdjCtrl value is nominal. TSSR < 0 because of ClkIn internal propagation delay TCPD.

After selection of port C, instead of selecting port D, the de-synchronization makes the port selection to restart on port A. Since port H was not selected, the data are not output to the ports but the last data (d1 to d8) are latched till next selection of port H. d9 to d16 are lost.

The synchronous reset ensures a re-synchronization of the port selection.

Figure 6-7. Synchronous Reset, 1:8 Ratio, DR Mode



6.4.5.2 Synchronous Reset, 1:4 Ratio, DR Mode

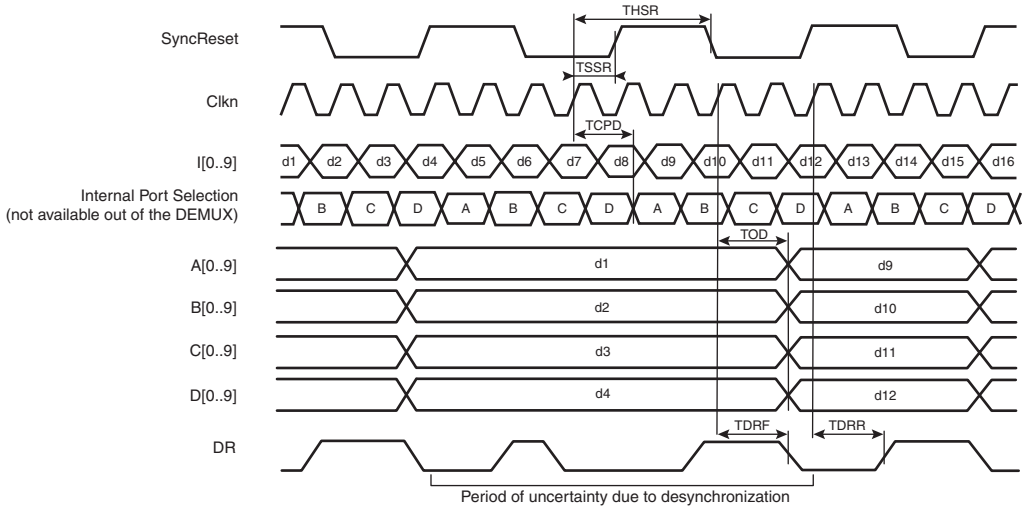
The desynchronization event happens after the selection of Port C.

DMUXDelAdjCtrl value is nominal. TSSR < 0 because of ClkIn internal propagation delay TCPD.

After selection of port C, instead of selecting port D, the de-synchronization makes the port selection to restart on port A. Since port D was not selected, the data are not output to the ports but the last data (d1 to d4) are latched till next selection of port D. d5 to d8 are lost.

The synchronous reset ensures a re-synchronization of the port selection.

Figure 6-8. Synchronous Reset, 1:4 Ratio, DR Mode



6.4.5.3 Synchronous Reset, 1:8 Ratio, DR/2 Mode

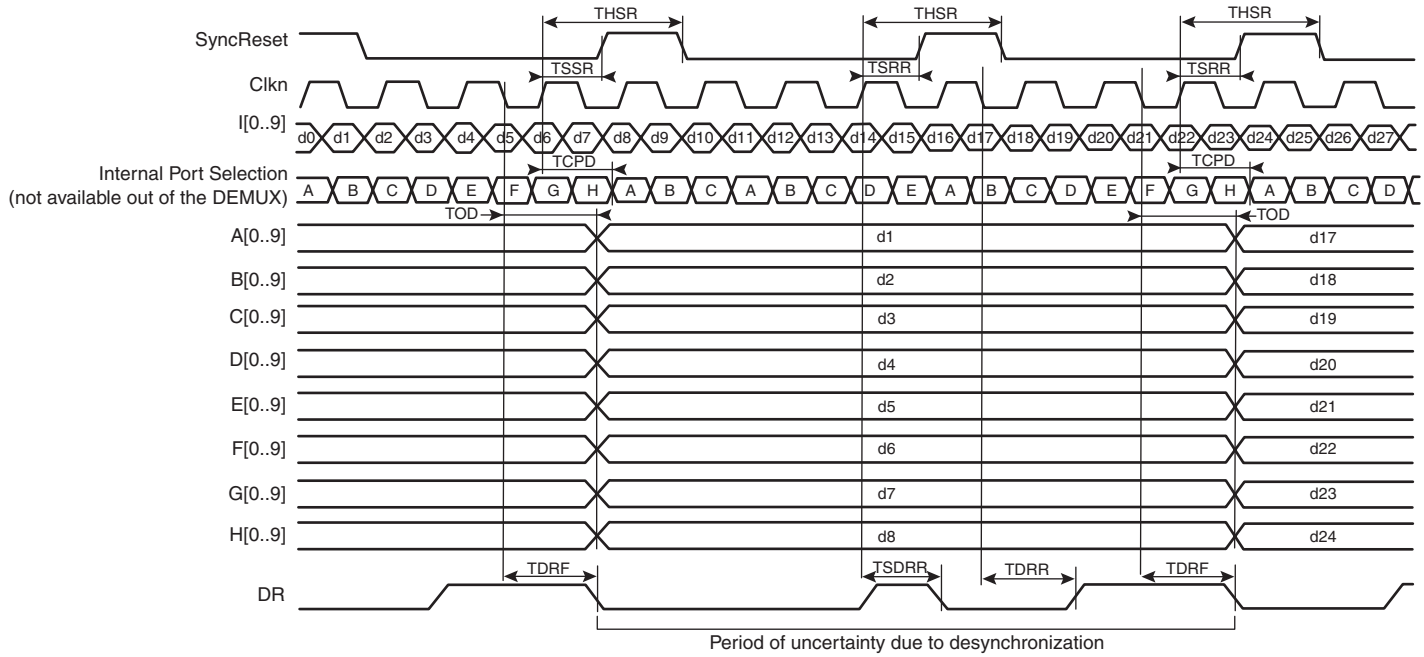
The desynchronization event happens after the selection of Port C.

DMUXDelAdjCtrl value is nominal. TSSR < 0 because of ClkIn internal propagation delay TCPD.

After selection of port C, instead of selecting port D, the de-synchronization makes the port selection to restart on port A. Since port H was not selected, the data are not output to the ports but the last data (d1 to d8) are latched till next selection of port H. d 9 to d16 are lost.

The synchronous reset ensures a re-synchronization of the port selection.

Figure 6-9. Synchronous Reset, 1:8 Ratio, DR/2 Mode

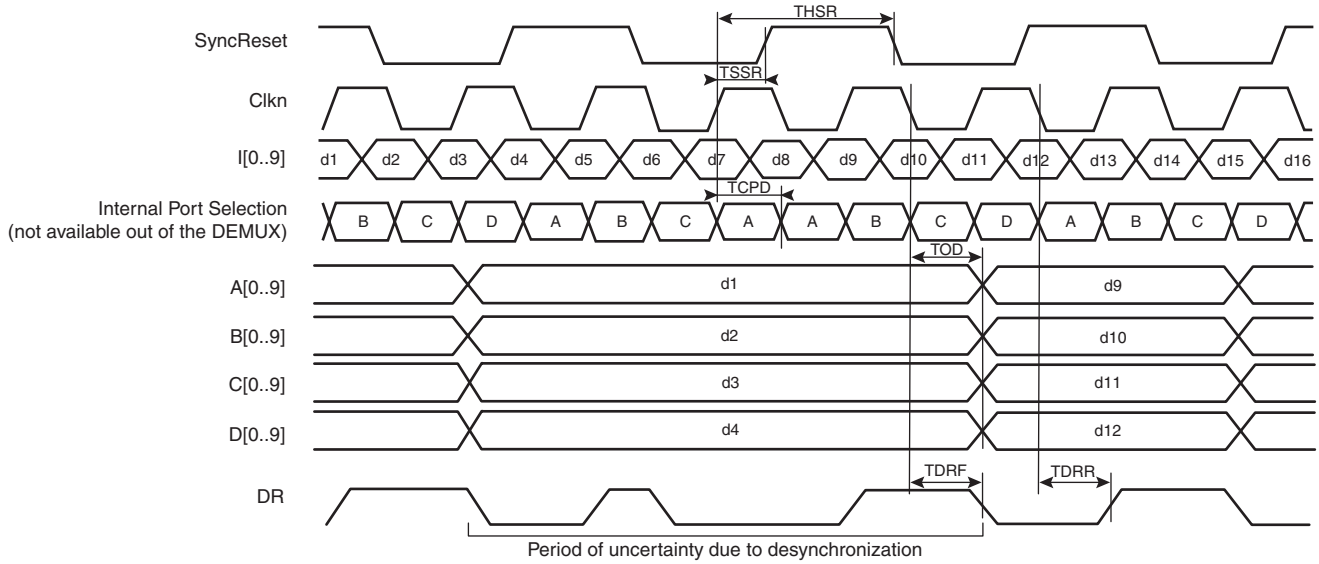


6.4.5.4 Synchronous Reset, 1:4 Ratio, DR/2 Mode

The desynchronization event happens after the selection of Port C.

DMUXDelAdjCtrl value is nominal. TSSR < 0 because of Clkln internal propagation delay TCPD.

Figure 6-10. Synchronous Reset, 1:4 Ratio, DR/2 Mode



After selection of port C, instead of selecting port D, the de-synchronization makes the port selection to restart on port A. Since port D was not selected, the data are not output to the ports but the last data (d1 to d4) are latched till next selection of port D. d5 to d8 are lost.

The synchronous reset ensures a re-synchronization of the port selection.

Note: In case of low clock frequency and start with asynchronous reset, only the first data is lost and the first data to be processed is the second one. This data goes out of the DEMUX by the port B.

7. Package Description

7.1 Function Description

Table 7-1. Pin Description

Type	Name	Levels	Comments
Digital Inputs	I[0…9]	Differential ECL	Data input. On-chip 100Ω differential termination resistor.
	ClkIn	Differential ECL	Clock input (Data Ready ADC). On-chip 100Ω differential termination resistor.
Outputs	A[0…9] → H[0…9]	Adjustable Logic Single	Data Ready for port A to H. Common mode is adjusted with V_{PLUSD}. Swing is adjusted with SwiAdj. 50Ω termination possible.
	DR	Adjustable Logic Differential	Data Ready for channel A to H. Common mode is adjusted with V_{PLUSD}. Swing is adjusted with SwiAdj. 50Ω termination possible.
	RefA → RefH	Adjustable Single	Reference voltage for output channels A to H. Common mode is adjustable with V_{PLUSD}. 50Ω termination possible.
Control Signals	ClkInType	TTL	Data Ready or Data Ready/2: logic 1:Data Ready.
	RatioSel	TTL	DMUX ratio; logic 1: 1:4
	Bist	TTL	Reset and Switch of built-in Self Test (BIST): logic 0: BIST active.
	SwiAdj	0V ± 0.5V	Swing fine adjustment of output buffers.
	Diode	Analog	Diode for chip temperature measurement.
	NbBit	TTL	Number of bit 8 or 10: logic 1: 10-bit.
Synchronization	AsyncReset	TTL	Asynchronous reset: logic 1: reset on.
	SyncReset	Differential ECL	Synchronous reset: active on rising edge.
	DMUXDelAdjCtrl	Differential analog input of ±0.5V around 0V common mode	Control of the delay line of Data Ready input: differential input = -0.5V: delay = 250 ps differential input = 0V: delay = 500 ps differential input = 0.5V: delay = 750 ps
	ADCDelAdjCtrl	Differential analog input of ±0.5V around 0V common mode	Control of the delay line for ADC: differential input = - 0.5V: delay = 250 ps differential input = 0V: delay = 500 ps differential input = 0.5V: delay = 750 ps
	ADCDelAdjIn	Differential ECL	Stand-alone delay adjust input for ADC. Differential termination of 100Ω inside the buffer.
	ADCDelAdjOut	50Ω differential output	Stand-alone delay adjust output for ADC.
Power Supplies	GND	Ground 0V	Common ground.
	V_{EE}	Power -5V	Digital negative power supply.
	V_{PLUSD}	Adjustable power from 0V to +3.3V	Common mode adjustment of output buffers.
	V_{CC}	Power +5V	Digital positive power supply.

7.2 Enhanced CQFP196 Package - Pin Description

Table 7-2. Pin Description

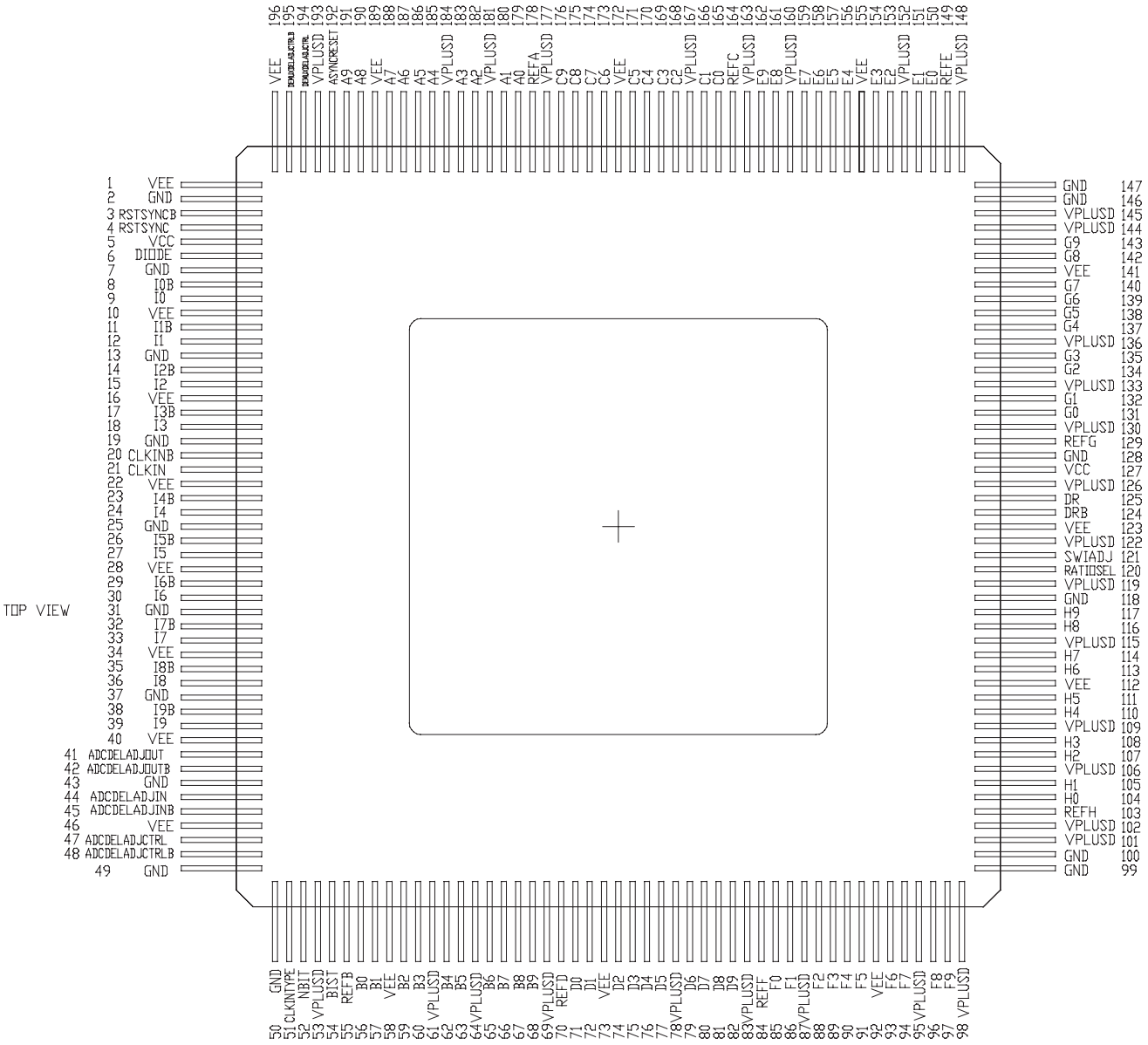
Symbol	Pin Number	Description
Power Supplies		
V_{CC}	5, 127	Positive +5V power Supply
V_{EE}	1, 10, 16, 22, 28, 34, 40, 46, 58, 73, 92, 112, 123, 141, 155, 172, 189, 196	Negative -5V power supply
V_{PLUSD}	53, 61, 64, 69, 78, 83, 87, 95, 98, 101, 102, 106, 109, 115, 119, 122, 126, 130, 133, 136, 144, 145, 148, 152, 160, 163, 167, 177, 181, 184, 193	Output buffer Power Supply
GND	2, 7, 13, 19, 25, 31, 37, 43, 49, 50, 99, 100, 118, 128, 146, 147	Ground
Analog Input Signals		
DMUXDelAdjCtrl	194	In phase DMUX Clock delay cell Control signal
DMUXDelAdjCtrlB	195	Inverted Phase DMUX Clock delay cell Control signal
ADCDelAdjCtrl	47	In phase Stand-alone delay cell Control signal
ADCDelAdjCtrlB	48	Inverted Phase Stand-alone delay cell Control signal
SwiAdj	121	Swing Adjust Function Control signal
DIODE	6	Die Junction Temperature Monitoring Signal
ECL Input Signals		
ClkIn	21	In phase Input Clock signal
ClkInB	20	Inverted Phase input clock signal
I[0…9]	9, 12, 15, 18, 24, 27, 30, 33, 36, 39	In phase input data
I[0…9]B	8, 11, 14, 17, 23, 26, 29, 32, 35, 38	Inverted Phase Input data
SyncReset	4	In phase Synchronous Reset
SyncResetB	3	Inverted Phase Synchronous Reset
ADCDelAdjIn	44	In phase Input of the stand-alone delay cell
ADCDelAdjInB	45	Inverted phase Input of the stand-alone delay cell
Output Data		
A[0…9] B[0…9] C[0…9] D[0…9] E[0…9] F[0…9] G[0…9] H[0…9]	179, 180, 182, 183, 185, 186, 187, 188, 190, 191 56, 57, 59, 60, 62, 63, 65, 66, 67, 68165, 166, 168, 169, 170, 171, 173, 174, 175, 176 71, 72, 74, 75, 76, 77, 79, 80, 81, 82150, 151, 153, 154, 156, 157, 158, 159, 161, 162 85, 86, 88, 89, 90, 91, 93, 94, 96, 97131, 132, 134, 135, 137, 138, 139, 140, 142, 143 104, 105, 107, 108, 110, 111, 113, 114, 116, 117	Output Data
RefA to RefH	178, 55, 164, 70, 149, 84, 129, 103	Reference outputs (tied to the common mode voltage of each port)

Table 7-2. Pin Description (Continued)

Symbol	Pin Number	Description
DR	125	In phase Data Ready Signal (centered in the output data, frequency = output data /2)
DRB	124	Inverted Phase Data Ready Signal (centered in the output data, frequency = output data /2)
TTL Input Signals		
ClkInType	51	Input clock type: - DR mode = Logic 1 - DR/2 mode = Logic 0
RatioSel	120	DMUX ratio selection: - 1:4 mode = Logic 1 - 1:8 mode = Logic 0
NbBit	52	Number of Bits selection: - 10 bits = Logic 1 - 8 bits = Logic 0
AsyncReset	192	Asynchronous Reset (Active High)
BIST	54	Built-In-Self Test Mode (active low)
Other Output Signals		
ADCDelAdjOUT	41	In phase Output of the stand-alone delay cell
ADCDelAdjOUTB	42	Inverted phase Output of the stand-alone delay cell

7.3 Enhanced CQFP 196 Pinout

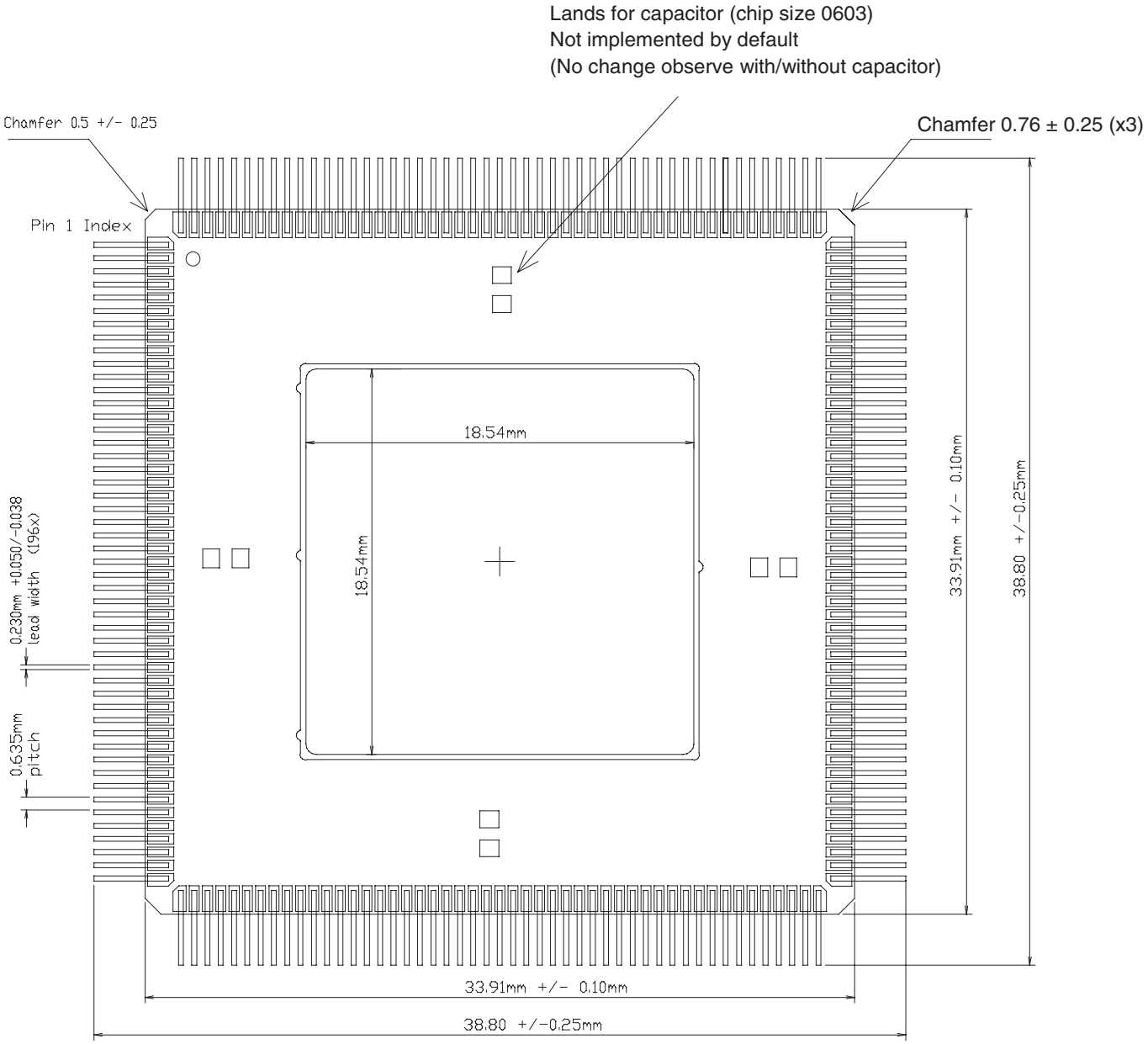
Figure 7-1. CQFP 196 Package Pinout



7.4 Outline Dimensions - CQFP 196

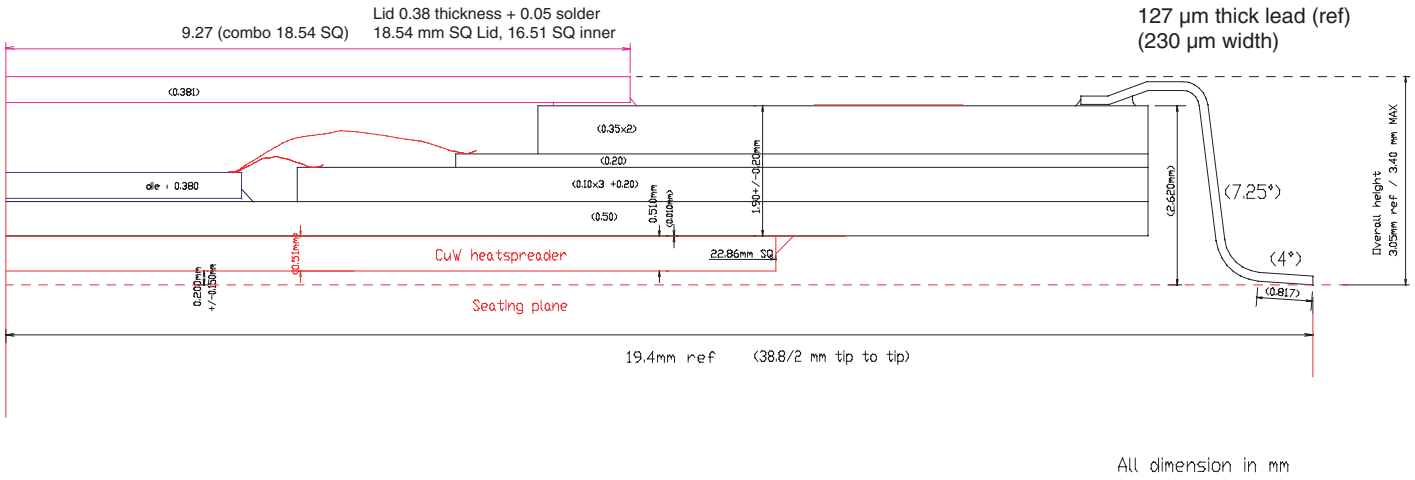
- Package: Black Al2O3 ceramic
- Leads: Kovar , Ni and Au plating
- Lid: Kovar , Ni and Au plating
- Heatspreader on bottom: CuW with Ni and Au plating

Figure 7-2. CQFP 196 Package Top View



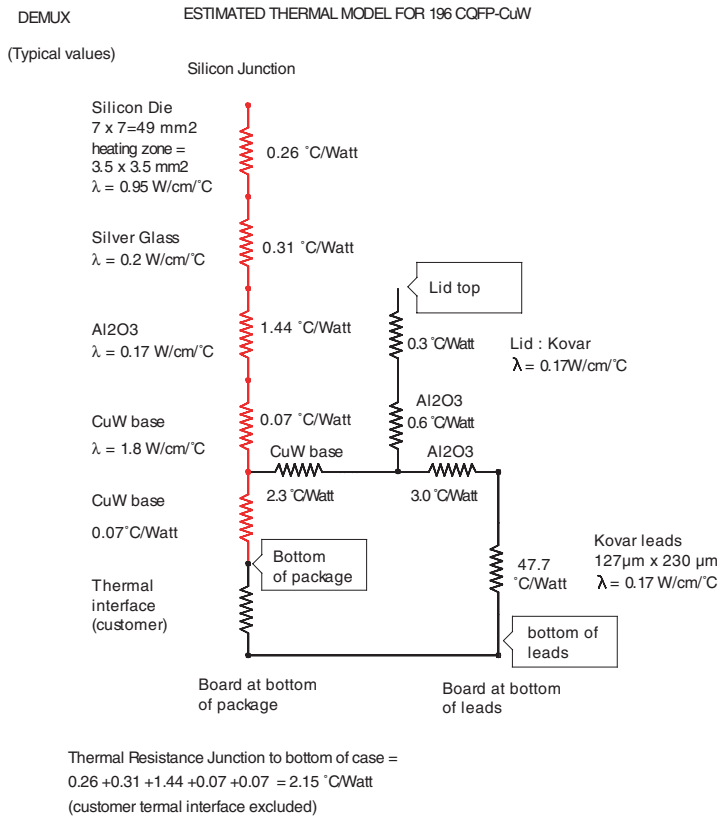
7.5 Detailed Cross Section

Figure 7-3. Detailed Cross Section



7.6 Thermal Characteristics

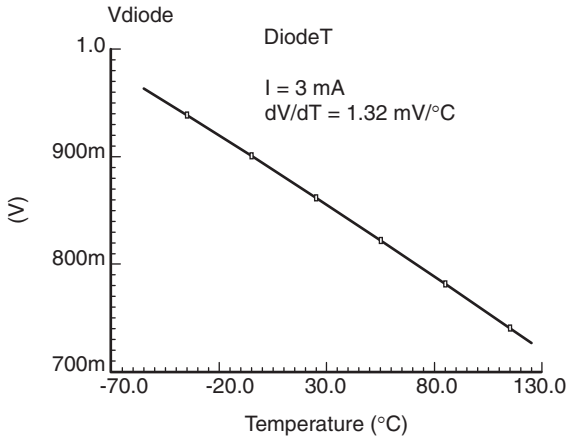
Figure 7-4. Thermal Characteristics



7.6.1 Temperature Diode Characteristics

The theoretical characteristic of the diode, in function of the temperature when I = 3 mA is depicted below:

Figure 7-5. Temperature Diode Characteristic



8. Ordering Information

Table 8-1.

Part Number	Package	Temperature Range	Screening	Comments
TS81102G0CFS	CQFP 196	"C" grade 0°C < T_C; T_J- < 90°C	Standard	
TS81102G0VFS	CQFP 196	"V" grade-40°C < T_C; T_J< 110°C	Standard	
TS81102G0MFS	CQFP 196	"M" grade-55°C < T_C; T_J< 125°C	Standard	
TS81102G0MFS9Nxy	CQFP 196	"M" grade-55°C < T_C; T_J< 125°C	- ESA/SCC9000 Screening - Non ESA/SCC qualified - x = B or C for respectively level B or C of ESA/SCC9000 - y = 1, 2 or 3 for respectively Lot Acceptance Test 1, 2 or 3	Please contact Marketing
TSEV81102G0FS	CQFP196	Ambient	Standard	Evaluation board

9. Datasheet Status Description

Table 9-1. Datasheet Status

Datasheet Status		**Validity**
Objective specification	This datasheet contains target and goal specifications for discussion with customer and application validation.	Before design phase
Target specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary specification α-site	This datasheet contains preliminary data. Additional data may be published later; could include simulation results.	Valid before characterization phase
Preliminary specification β-site	This datasheet contains also characterization results.	Valid before the industrialization phase
Product specification	This datasheet contains final product specification.	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification.		

9.1 Life Support Applications

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