

1. INTRODUCTION

This note describes an issue seen with the SYNC and the POR function on EV1xDS130 revision A (EV1xDS130A). This issue has been fixed on EV1xDS130 revision B (EV1xDS130B).

It gives some recommendations for workarounds.

This document applies to the following parts and their evaluation boards:

- EV10DS130Axxxx 10-bit 3Gsps DAC
- EV12DS130Axxxx 12-bit 3Gsps DAC
- EVX10DS130Axxxx 10-bit 3Gsps DAC
- EVX12DS130Axxxx 12-bit 3Gsps DAC

This document must be read with the latest datasheet version available on the following URL depending on the part targeted:

EV10DS130A/BZP: <http://www.e2v.com/products/ev10ds130/>

EV10DS130A/BG: <http://www.e2v.com/products/ev10ds130-b/>

EV12DS130A/BZP: <http://www.e2v.com/products/ev12ds130/>

EV12DS130A/BG: <http://www.e2v.com/products/ev12ds130-b/>

For further assistance please contact hotline-bdc@e2v.com

2. DESCRIPTION OF PROBLEM

When using the SYNC feature, special care should be taken to guarantee safe operation of the DAC.

The SYNC could be initiated:

- On command with the external differential SYNC input;
- On power-up with the internal POR (Power On Reset).

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3. POSSIBLE SOLUTIONS

3.1 No SYNC function is required in the application

The 2 following cases can be used depending on their implementation easiness.

3.1.1 Case 1

1. To ensure that no external SYNC could be generated:
 - SYNCN pin should be pull-up at Vcca3 via a 1500 ohms resistor.
 - SYNCP pin should be pull-down via a 910 ohms resistor.
2. To ensure an internal SYNC pulse is NOT generated during the power up, it is necessary to respect the following supply sequence:
 - VCCA5,
 - VCCA3,
 - And Finally VCCD.

It is mandatory that VCCD is the last supply to rise and always remains behind the VCCA5 and VCCA3.

3. It is mandatory to merge AGND and DGND ground planes.

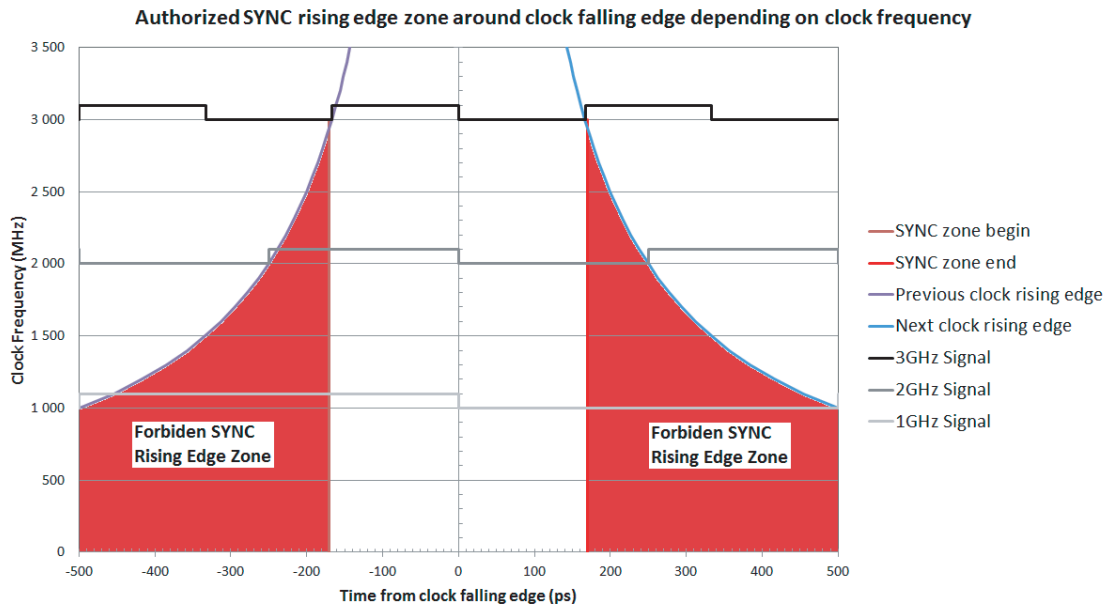
3.1.2 Case 2

1. To ensure that no external SYNC could be generated:
 - SYNCN pin should be pull-up at Vcca3 via a 1500 ohms resistor.
 - SYNCP pin should be pull-down via a 910 ohms resistor.
2. VCCA3 must be higher than VCCD by 150mV
3. DGND and AGND ground plane must be merged

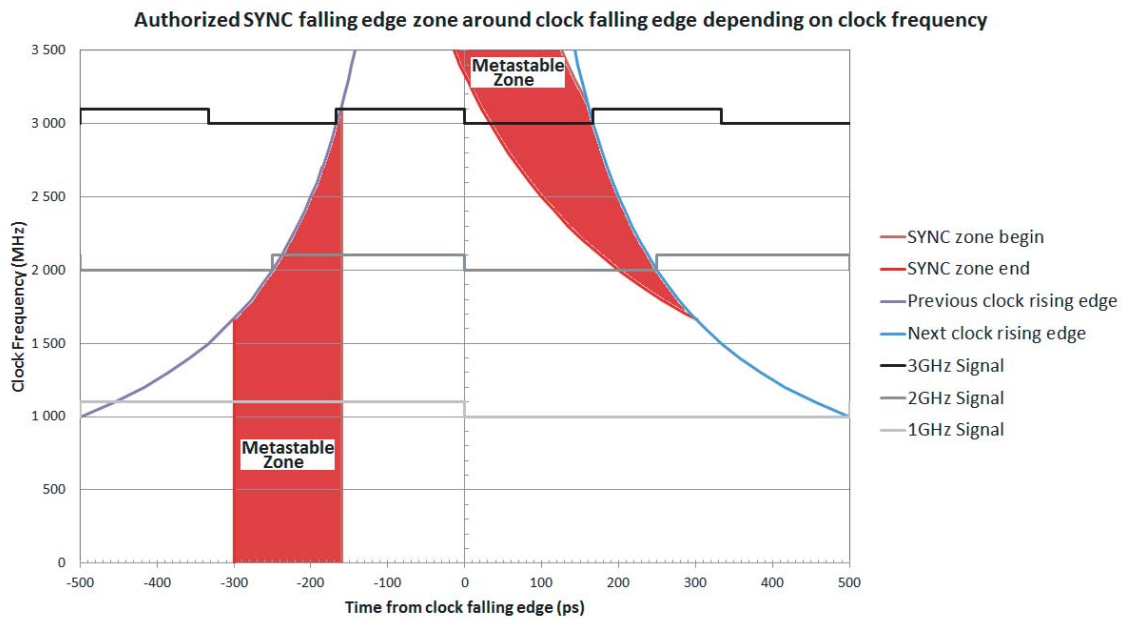
3.2 SYNC function is required in the application

External SYNC pins can be used to generate a SYNC but it is mandatory to respect some constraints to avoid any problem:

1. The SYNC signal should be applied via LVDS SYNCP and SYNCN pins. It should be synchronous with the external clock.
2. It is mandatory that VCCA3 is 150mV higher than VCCD.
3. It is mandatory to merge AGND and DGND ground planes.
4. To correctly perform the synchronization procedure, the rising edge SYNC pulse should be synchronized with the falling edge of the clock.
The rising edge of the SYNC signal must be applied into a ± 170 ps window around falling edge of the clock as shown on the following diagram.



5. To correctly perform the synchronization procedure, the falling edge SYNC pulse should be synchronized with the falling edge of the clock. The falling edge of the SYNC signal must be applied avoiding the 300ps-160ps window before the falling edge of the clock as shown on the following diagram.



For any question, please contact hotline-bdc@e2v.com.

4. REVISION HISTORY

This table provides revision history for this document.

Table 4-1. Revision History

Rev. No	Date	Substantive Change(s)
1125C	10/2015	Release on e2v website Section 3.2 modified to make the 2 options more visible; Section 3.2 removed voltage relation between power supplies during power-up sequence
1125BX	10/2013	Introduction: part number list updated SYNC function is required in the application: updated (0.5V instead of 1.0V)
1125AX	09/2013	Initial revision