CCD42-40 NIMO Back Illuminated High Performance CCD Sensor

FEATURES

- 2048 by 2048 pixel format
- 13.5 µm square pixels
- Image area 27.6 x 27.6 mm
- Back Illuminated format for high quantum efficiency
- Full-frame operation
- Symmetrical anti-static gate protection
- Very low noise output amplifiers
- Dual responsivity output amplifiers
- Wide dynamic range for 15-bit operation
- Gated dump drain on output register
- 100% active area
- New compact footprint package

APPLICATIONS

- Scientific Imaging
- Microscopy
- Medical Imaging
- Astronomy

INTRODUCTION

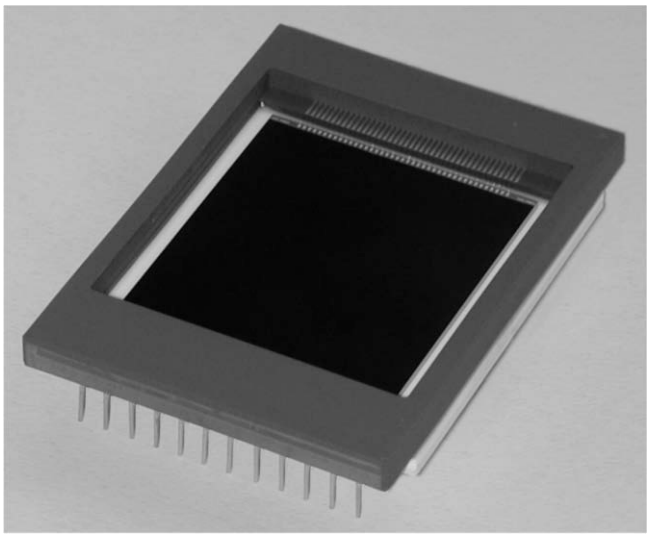
This version of the CCD42 family of CCD sensors has full-frame architecture. Back illumination technology, in combination with extremely low noise amplifiers, makes the device well suited to the most demanding applications requiring a high dynamic range. To improve the sensitivity further, the CCD is manufactured without anti-blooming structures. The CCD is available with either standard or deep depleted silicon.

There are two low noise amplifiers in the read out register, one at each end. Charge can be made to transfer through either or both amplifiers by making the appropriate RØ connections. The readout register has a gate controlled dump drain to allow fast dumping of unwanted data.

The register is designed to accommodate four image pixels of charge and a summing well is provided capable of holding six image pixels of charge. The output amplifier has a feature to enable the responsivity to be reduced, allowing the reading of such large charge packets.

Other variants of the CCD42-40 available are front illuminated format and inverted mode. In common with all e2v technologies CCD Sensors, the front illuminated CCD42-40 can be supplied with a fibre-optic window or taper, or with a phosphor coating.

Designers are advised to consult e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

(Low noise mode)

Pixel readout frequency	45 kHz
Output amplifier sensitivity	4.5 µV/e^-
Peak signal	150 ke^-/pixel
Dynamic range @ 18 kHz	50000:1
Spectral range	200–1060 nm
Readout noise @ 18 kHz	3 e^- rms
Peak output voltage	675 mV

GENERAL DATA

Format

Image area	27.6 x 27.6 mm
Active pixels	2048 (H) x 2048+4 (V)
Pixel size	13.5 x 13.5 µm
Number of output amplifiers	2
Number of underscan (serial) pixels	50

Package

Package size	37.0 x 51.7 mm
Number of pins	24
Inter-pin spacing	2.54 mm
Inter-row spacing	45.72 mm
Window material	Removable glass
Package type	Ceramic DIL array

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PERFORMANCE

			Min	Typical	Max	Units	Note
Peak charge storage			80,000	150,000		e^-/pixel	1
Peak output voltage (unbinned)				675		mV	3
Dark signal at 293 K	Standard Silicon			20,000	45,000	e^-/pixel/s	2, 8
Dark signal at 153 K	Deep Depleted Silicon			0.2	1	e^-/pixel/hr	2, 7
Charge transfer efficiency		Parallel	99.999	99.9999	-	%	4
		Serial	99.999	99.9993	-	%	
Output amplifier responsivity	Low noise mode		3	4.5	6	µV/e^-	
	High signal mode			1.5			3
Readout noise	Low noise mode			3	4	rms e^-/pixel	5
	High signal mode			6		rms e^-/pixel	3
Readout frequency				45	3000	KHz	6
Output node capacity				1,000,000		e^-	3, 9
Output Non-Linearity			-1.5	-	+1.5	%	11

SPECTRAL RESPONSE

Standard Silicon at 238K (-35C)

Wavelength (nm)	Minimum Response (QE) (see note 10)							Maximum Response Non-uniformity (1σ)	
	Enhanced Process UV Coated	Enhanced Process Uncoated	Enhanced Process Broadband Coated	Enhanced Process Midband Coated	Basic Process Midband Coated	Basic Process Broadband Coated	Basic Process Uncoated		
300	45	25	-	-	-	-	-	-	%
350	45	30	50	25	15	25	10	-	%
400	55	40	80	50	40	55	25	3	%
500	60	50	80	85	85	75	55	-	%
650	60	55	75	85	85	75	50	3	%
900	30	28	30	30	30	30	28	5	%

Deep Depleted Silicon at 188K (-85C)

Wavelength (nm)	Minimum Response (QE)				Maximum Response Non-uniformity (1σ)	
	Enhanced Process Broadband Coated	Basic Process NIR (ER1 900 nm) Coated	Astronomy Process Multilayer 2 Coated	Basic Process Uncoated		
300	-	-	-	-	-	%
350	40	-	30	10	-	%
400	70	25	75	25	3	%
500	75	45	75	50	-	%
650	70	75	80	55	3	%
900	40	45	50	40	5	%

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances (Measured at mid-clock level)

	Min	Typical	Max	
I∅/I∅ interphase	-	16	-	nF
I∅/SS	-	32	-	nF
R∅/R∅ interphase	-	80	-	pF
R∅/(SS + DG + OD)	-	150	-	pF
Output impedance at typical operating conditions	-	350	-	Ω

NOTES

1. Signal level at which resolution begins to degrade. The typical values are those expected from design.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 K and 300 K may be estimated from:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

   where Q□d0□ is the dark signal at 293 K.
3. Not production tested at factory.
4. CCD measurements made using charge generated by X-ray photons of known energy.
5. Measured at a pixel readout frequency of 18 KHz using a dual-slope integrator technique (i.e. correlated double sampling). All other tests measured at 45 KHz.
6. Readout above 3 MHz can be achieved but performance to the parameters given cannot be guaranteed.
7. Measured at 188K, excluding white defects with substrate at 3V
8. Measured at 238K, excluding white defects with substrate held high.
9. With output circuit configured in low responsivity/high capacity mode (OG2 high).
10. The uncoated process is suitable for soft X-ray and EUV applications.
11. Non-Linearity measured over the signal range 20-150ke with pixel binning.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- .

Black spots Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 20 times the specified maximum dark signal generation rate (measured between 243 and 293 K). The typical temperature dependence of white spot blemishes is the same as that of the average dark signal i.e.:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

Column defects A column which contains at least 50 white or 50 black defects.

Standard Silicon

GRADE	0	1	2
Column defects; black or white	0	3	6
Black spots	100	150	250
Traps >200 e^-	10	20	30
White spots	100	150	200

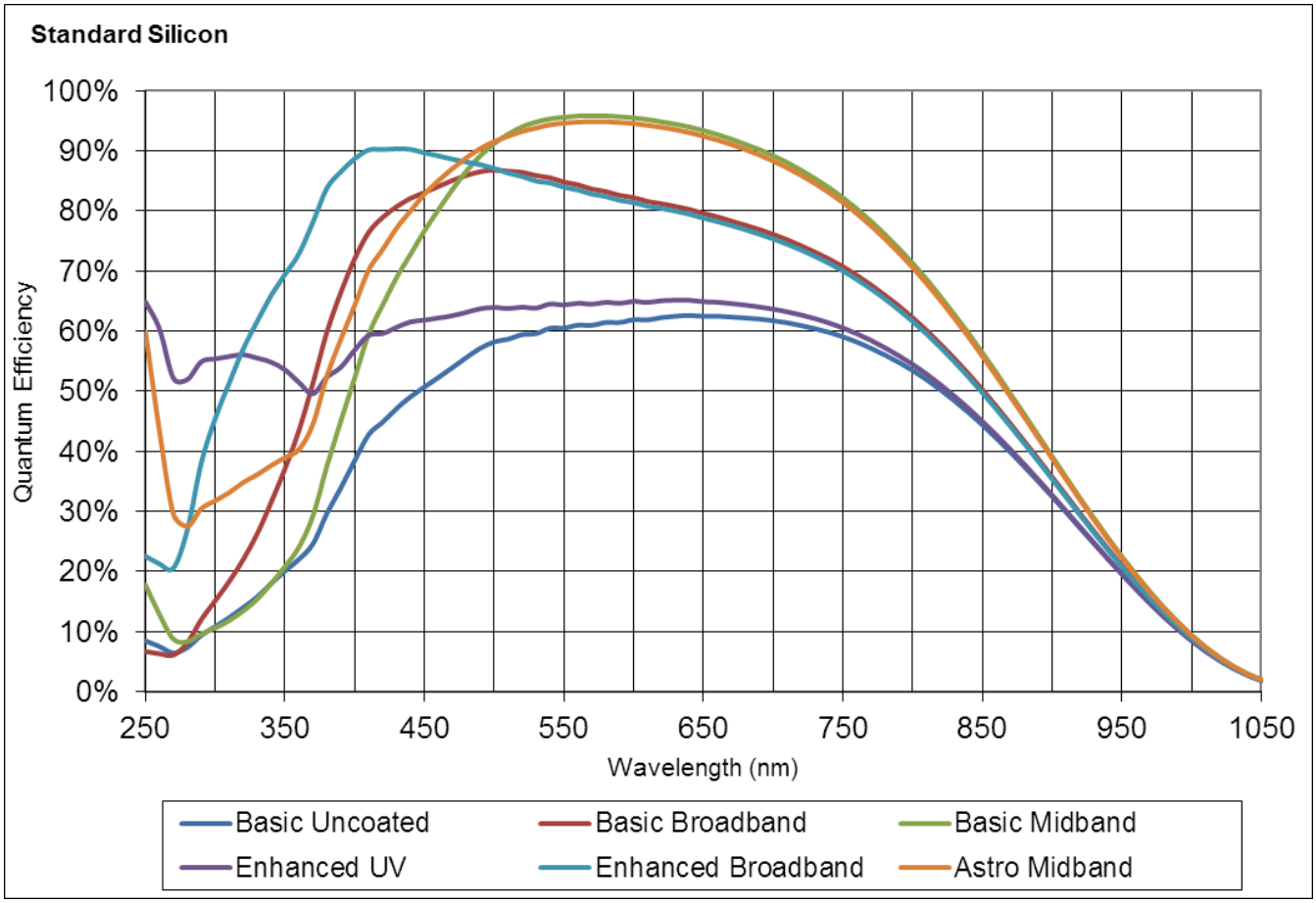
Deep Depleted Silicon

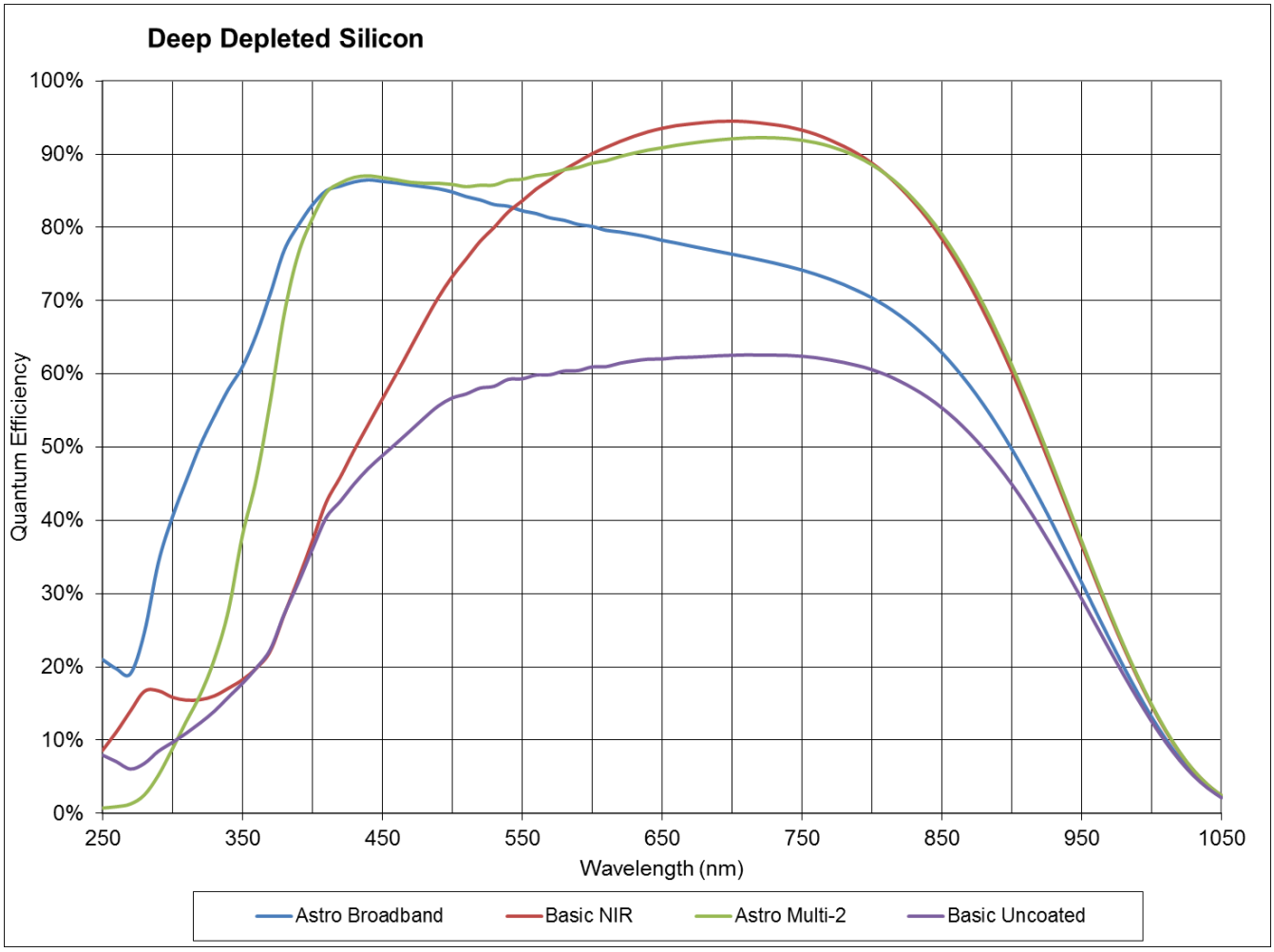
GRADE	0	1	2
Column defects; black or white	3	6	10
Black spots	250	500	1000
Traps >200 e^-	20	30	40
White spots	250	500	800

Grade 5 Devices which are fully functional, with image quality below that of grade 2, and which may not meet all other performance parameters.

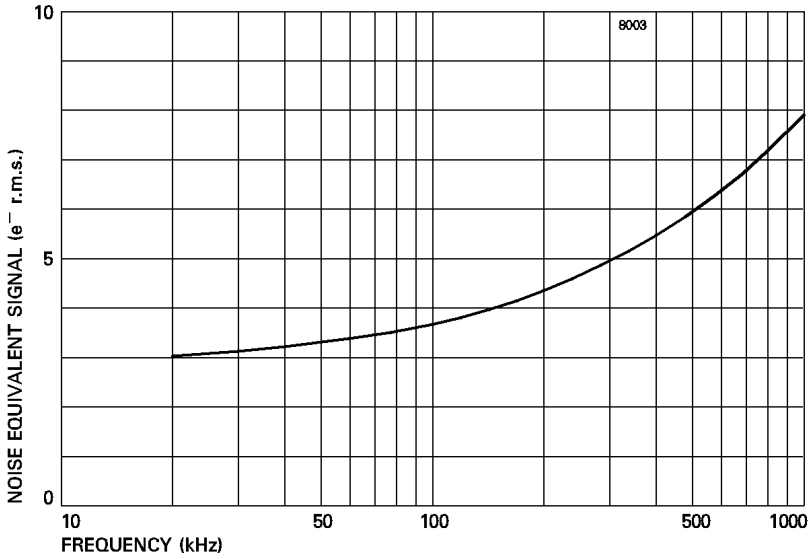
Note: The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 243 K. The amplitude of white spots and columns will decrease rapidly with temperature.

TYPICAL SPECTRAL RESPONSE (At –35 °C for Standard Silicon, –85 °C for Deep Depleted Silicon)

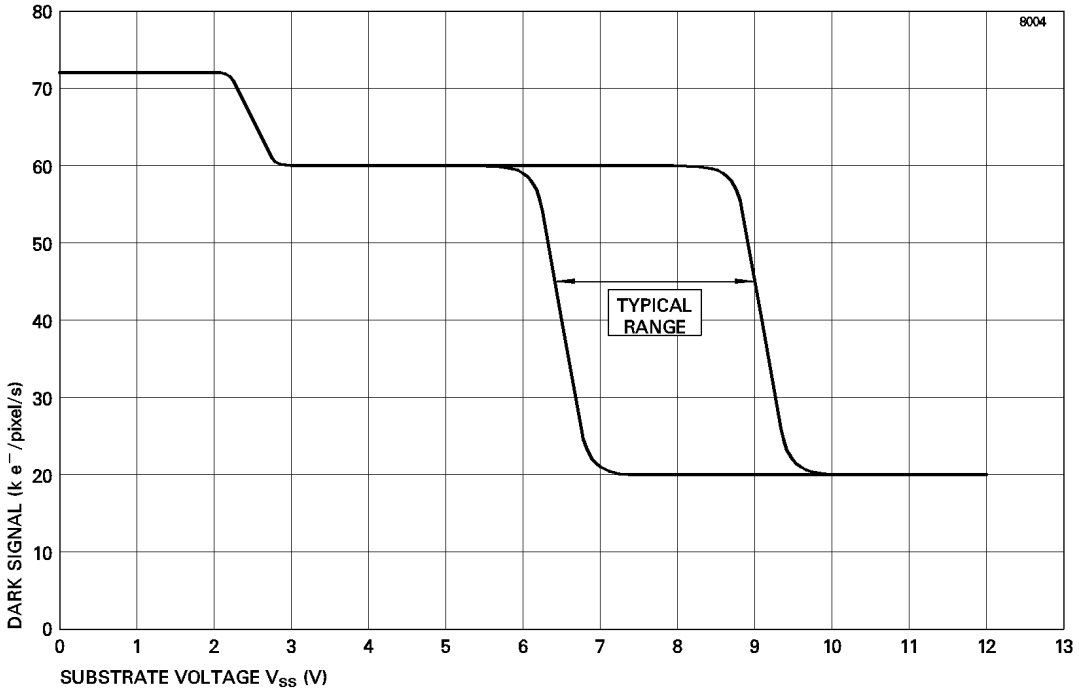




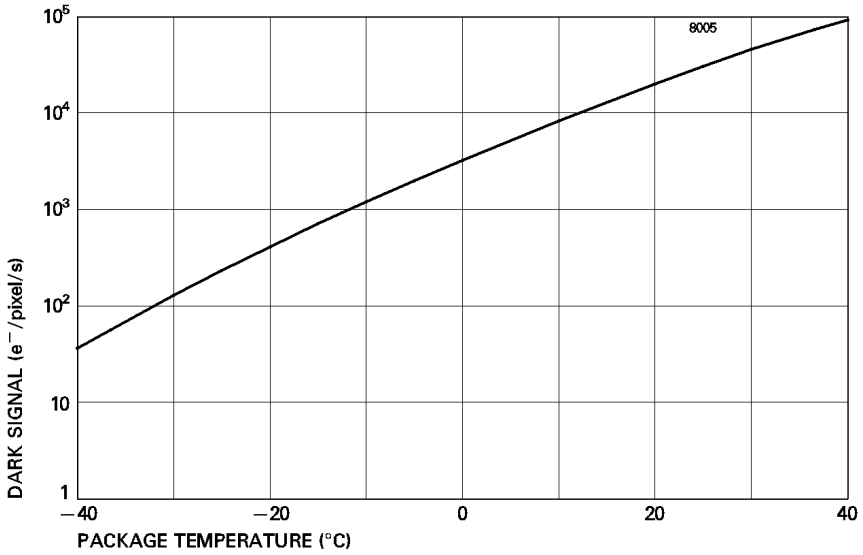
TYPICAL OUTPUT CIRCUIT NOISE (If Measured using clamp and sample)



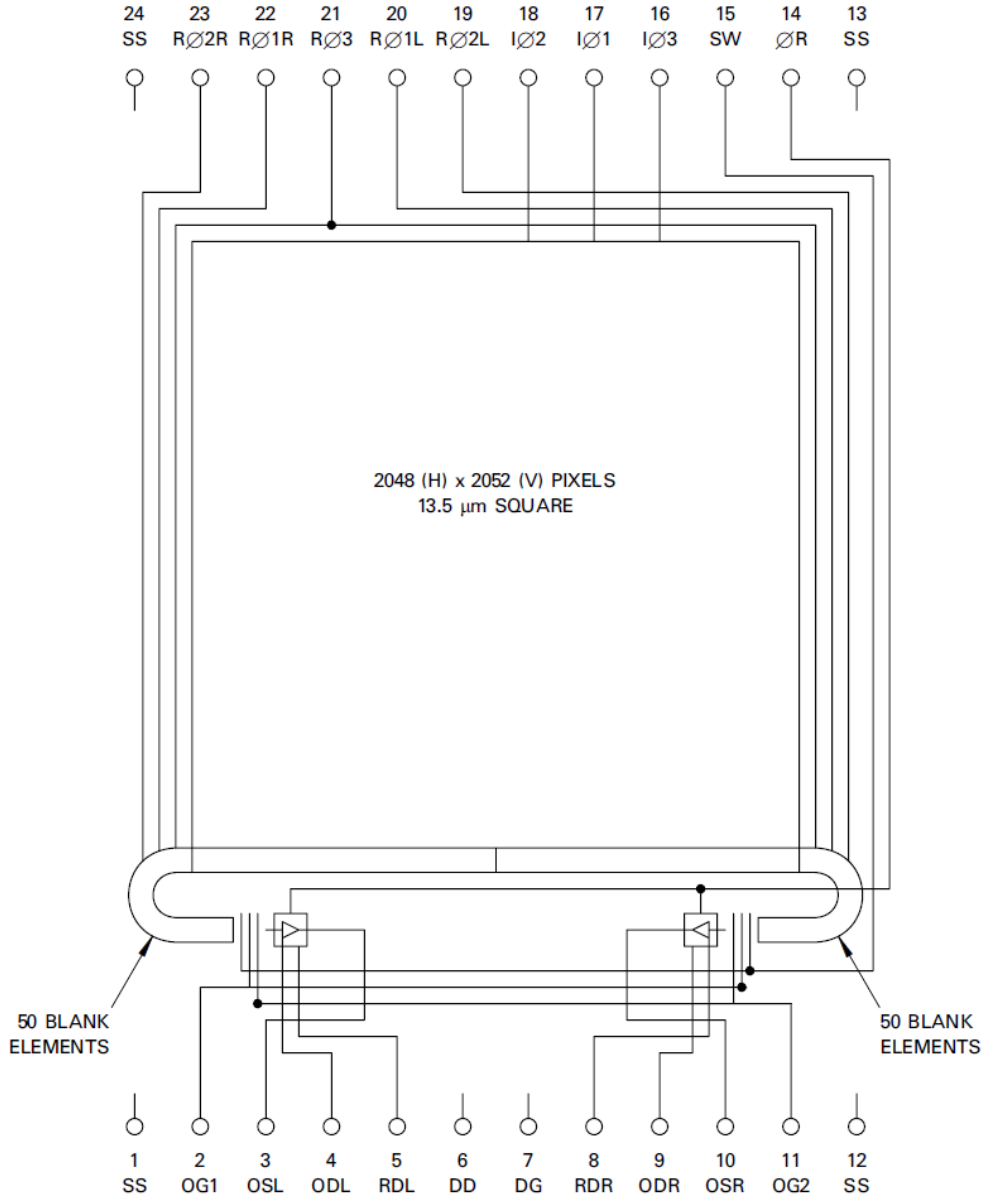
TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE at 293K



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	CLOCK LOW Typical	CLOCK HIGH OR DC LEVEL (V)			MAXIMUM RATINGS with respect to V_{SS}
				Min	Typical	Max	
1	SS	Substrate (see note 12)	n/a	0	9	10	-
2	OG1	Output gate 1	n/a	2	3	4	±20 V
3	OSL	Output transistor source (left)	n/a	see note 13			–0.3 to +25 V
4	ODL	Output drain (left)	n/a	27	29	31	–0.3 to +32 V
5	RDL	Reset drain (left)	n/a	15	17	19	–0.3 to +25 V
6	DD	Dump drain	n/a	22	24	26	–0.3 to +30 V
7	DG	Dump gate (see note 14)	0	-	12	15	±20 V
8	RDR	Reset drain (right)	n/a	15	17	19	–0.3 to +25 V
9	ODR	Output drain (right)	n/a	27	29	31	–0.3 to +32 V
10	OSR	Output transistor source (right)	n/a	see note 13			–0.3 to +25 V
11	OG2	Output gate 2 (see note 15)	4	16	20	24	±25 V
12	SS	Substrate	n/a	0	9	10	-
13	SS	Substrate	n/a	0	9	10	-
14	∅R	Reset gate	0	8	12	15	±20 V
15	SW	Summing well		Clock as R∅3			±20 V
16	I∅3	Image area clock, phase 3	0	8	10	15	±20 V
17	I∅1	Image area clock, phase 1	0	8	10	15	±20 V
18	I∅2	Image area clock, phase 2	0	8	10	15	±20 V
19	R∅2L	Register clock phase 2 (left)	1	8	11	15	±20 V
20	R∅1L	Register clock phase 1 (left)	1	8	11	15	±20 V
21	R∅3	Register clock phase 3	1	8	11	15	±20 V
22	R∅1R	Register clock phase 1 (right)	1	8	11	15	±20 V
23	R∅2R	Register clock phase 2 (right)	1	8	11	15	±20 V
24	SS	Substrate	n/a	0	9	10	-

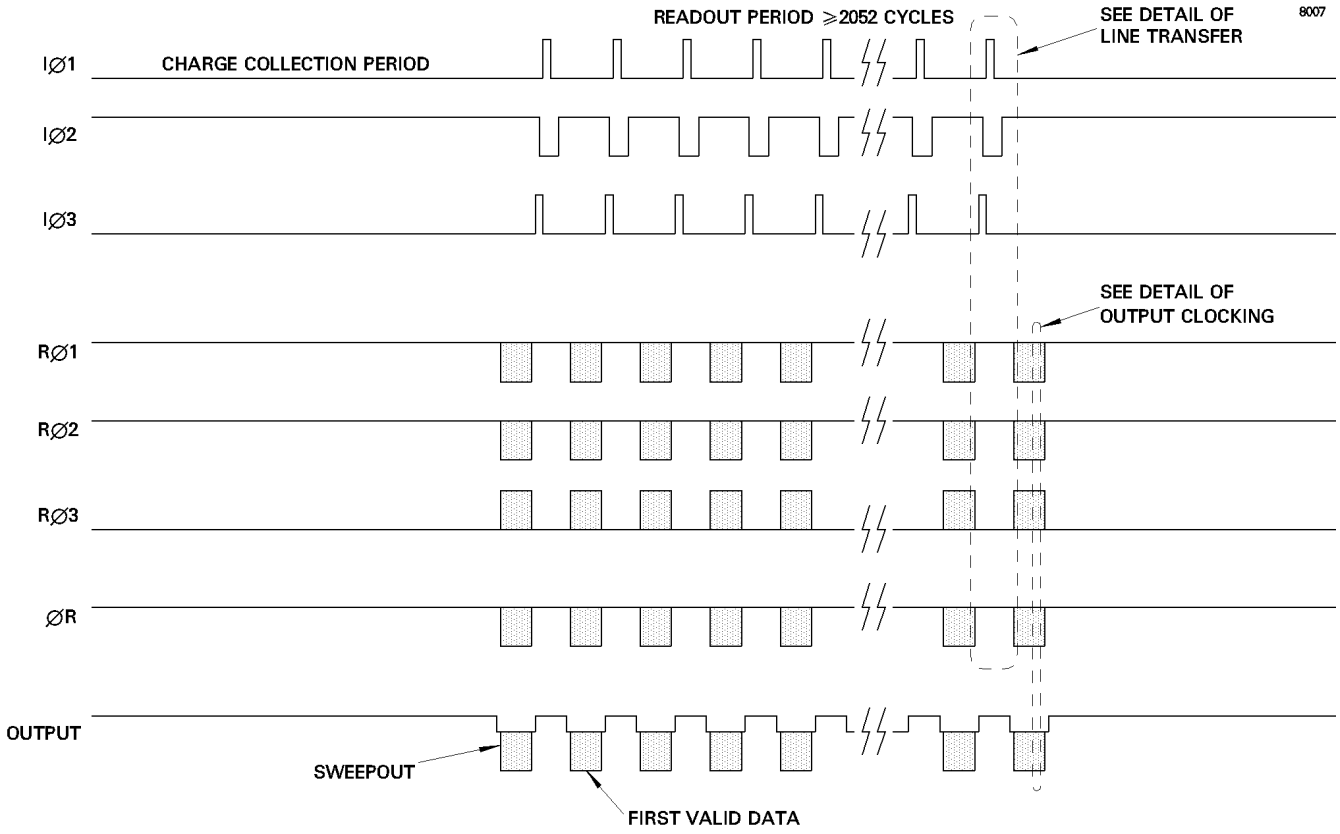
If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimise performance. Refer to the specific device test data if possible.

Maximum voltages between pairs of pins:
pin 3 (OSL) to pin 4 (ODL) ..... +15 V
pin 9 (ODR) to pin 10 (OSR) ..... +15 V
Maximum output transistor current ..... 10 mA

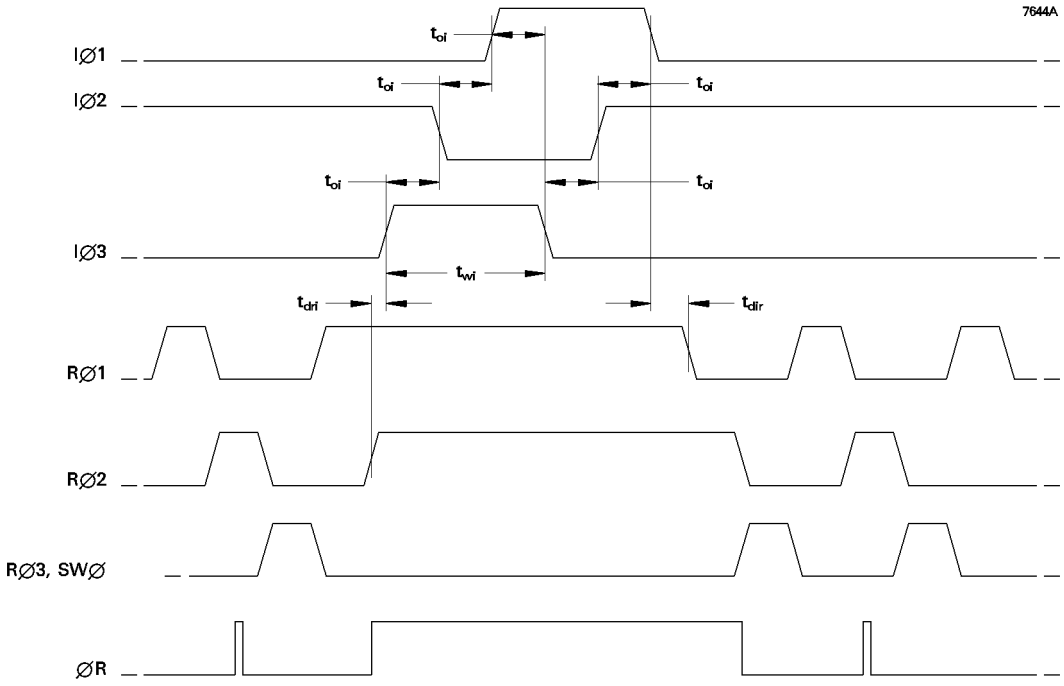
NOTES

12. Standard silicon variants are tested with high substrate (9 V). Deep depletion variants are tested colder and with low substrate (3 V).
13. Not critical; OS = 3 to 5 V below OD typically. Connect to ground using a 3 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).
14. This gate is normally low. It should be pulsed high for charge dump.
15. OG2 = OG1 + 1 V for operation of the output in high responsivity, low noise mode. For operation at low responsivity, high signal, OG2 should be set high.
16. With the R∅ connections shown, the device will operate through both outputs simultaneously. In order to operate from the left output only, R∅1(R) and R∅2(R) should be reversed.

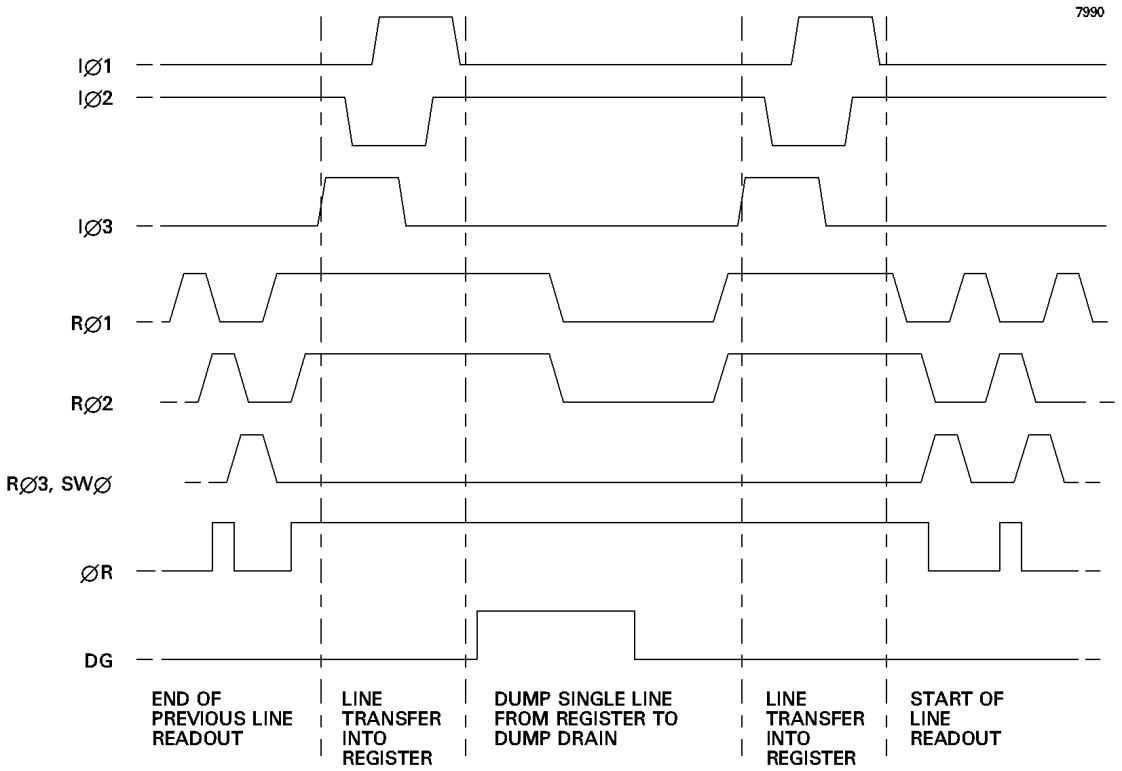
FRAME READOUT TIMING DIAGRAM



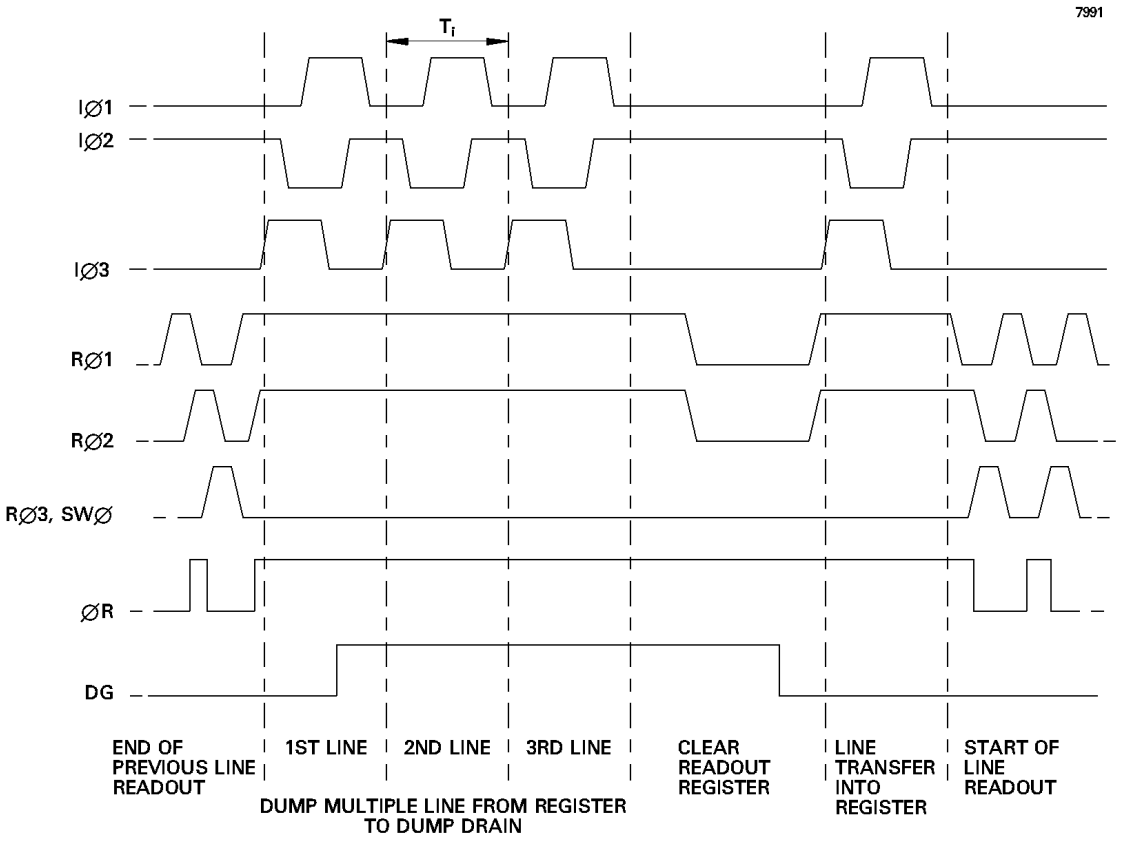
DETAIL OF LINE TRANSFER (Not to scale)



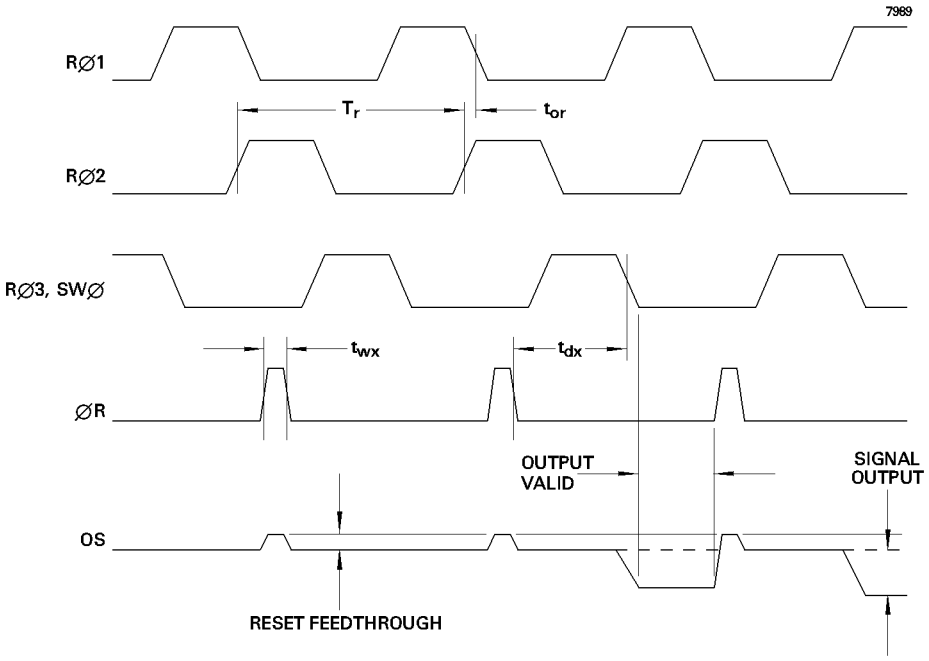
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



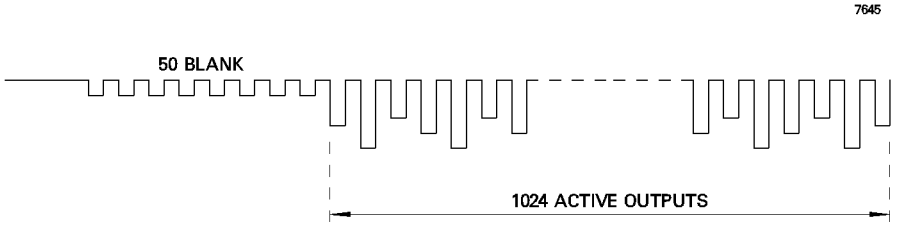
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING (Operation through both outputs)



LINE OUTPUT FORMAT (Split read-out operation)



CLOCK TIMING REQUIREMENTS

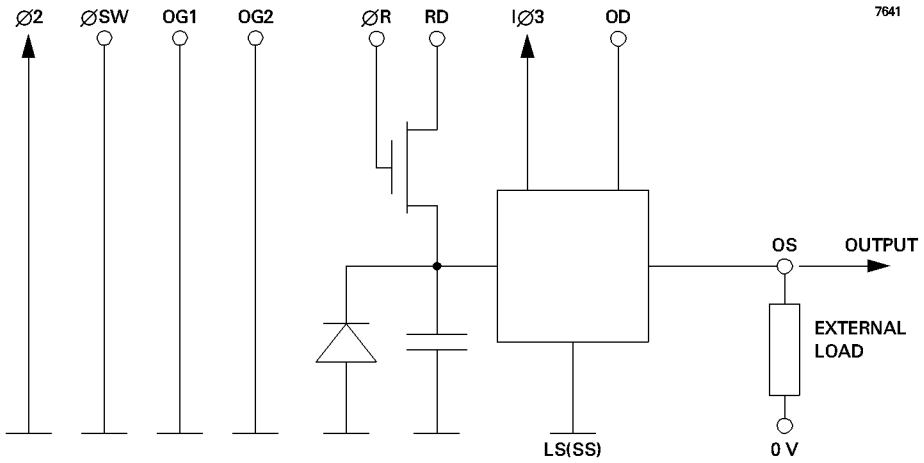
Symbol	Description	Min	Typical	Max	
T_i	Image clock period	10	20	see note 17	µs
t_{wi}	Image clock pulse width	5	10	see note 17	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	2	$0.2T_i$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$0.2T_i$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri} + t_{fi})/2$	2	$0.2T_i$	µs
t_{dir}	Delay time, I∅ stop to R∅ start	3	5	see note 17	µs
t_{dri}	Delay time, R∅ stop to I∅ start	1	2	see note 17	µs
T_r	Output register clock cycle period	300	see note 18	see note 17	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

17. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

18. As set by the readout period.

OUTPUT CIRCUIT



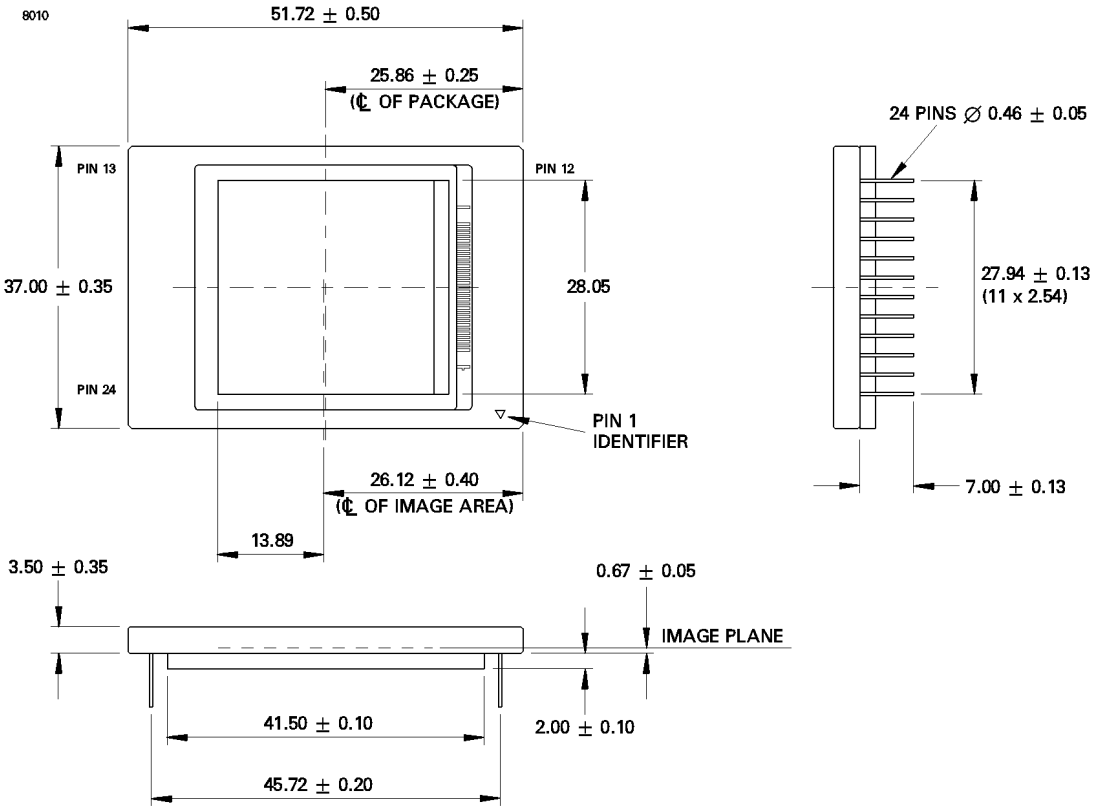
NOTES

19. The amplifier has a DC restoration circuit which is internally activated whenever I∅3 is high.

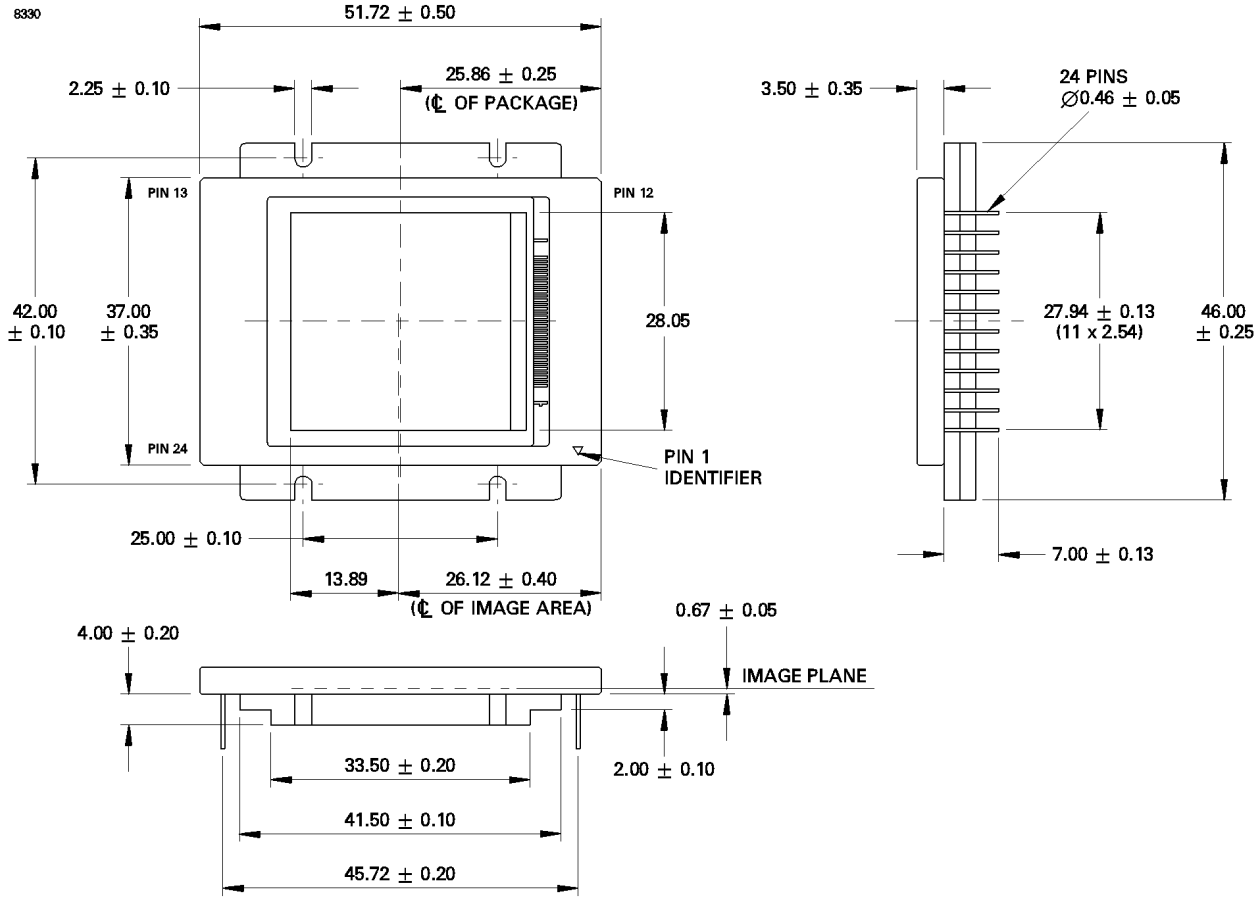
20. External load not critical; can be a 3 to 5 mA constant current supply or an appropriate load resistor.

OUTLINES (All dimensions in millimetres; dimensions without limits are nominal)

Standard Ceramic Package



Metal Base Package (available to special order)



ORDERING INFORMATION

Options include:

- Temporary quartz window
- Temporary glass window
- Fibre-optic coupling
- UV coating
- X-ray phosphor coating

For further information on the performance of these and other options, contact e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 7, 11, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Certain characterisation data are held at e2v technologies. Users planning to use CCDs in a high radiation environment are advised to contact e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	-	373	K
Operating	153	243	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling .....5 K/min