

# Analysis of Near-Field Diffraction Effects on CCD Resolution

D. Logan<sup>1</sup>, S. McFaul<sup>1</sup>, P.E. Jessop<sup>1</sup>, A.P. Knights<sup>1</sup>, M. Ledgerwood<sup>2</sup>, N. O<sup>2</sup>

<sup>1</sup> Department of Engineering Physics, McMaster Univ., Hamilton, ON, Canada L8S 4L7. fax: (905)527-8409 telephone: (905)525-9140 x24928

<sup>2</sup> Dalsa, Inc., 605 McMurray Rd. Waterloo, ON, Canada N2V 2E9.

e-mail: [logand@mcmaster.ca](mailto:logand@mcmaster.ca)

**Abstract:** The limitations in CCD pixel size reduction resulting from diffraction by fine structures close to the pixel surface is investigated using RSoft's FullWAVE simulation software. Cross-talk between small-size pixels was reduced by decreasing the collection depth or the distance between the fine structures and the CCD surface.

## 1. Introduction

A problem encountered as pixel size in a CCD imaging array is reduced is diffraction caused by fine structures above the pixel surface, which can lead to cross-talk between adjacent pixels and limit the overall resolution. This effect was investigated for front side illuminated CCDs, where diffraction from metal wires is a potential problem.

## 2. Experimental Results and Discussion

This investigation was implemented through simulations using RSoft's FullWAVE, an FDTD software package capable of numerically solving Maxwell's equations in a structure drawn in a CAD environment. The structure is shown as Figure 1, and consists of a silicon absorbing region, with metal lines lying one micron from the silicon, directly over the pixel isolation region.

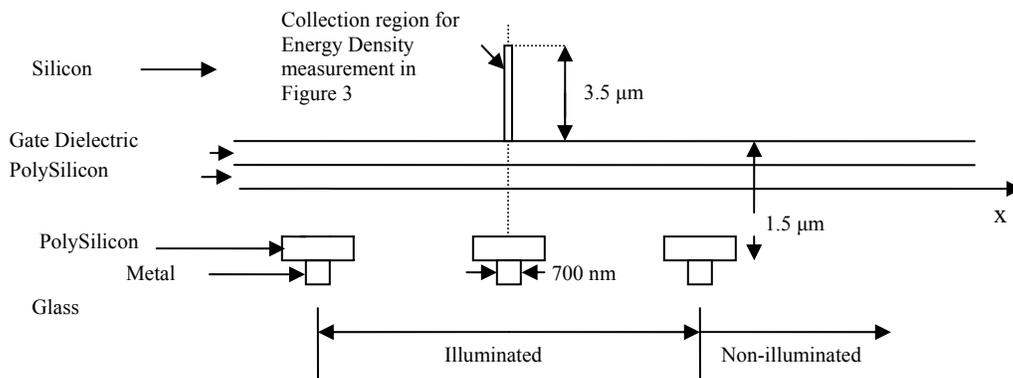


Figure 1: Single Metal Structure used to model diffraction effects on CCD pixels.

In the first simulation, two pixels were entirely illuminated with 600 nm and 800 nm plane wave input light. The energy density in an adjacent non-illuminated pixel was measured (integrated from the silicon surface to a depth of 3.5 μm), and compared to that measured in the fully illuminated pixel. The ratio of the two values was measured for pixel widths of 2.5 μm to 10 μm, and is plotted as Figure 2. It was found that the non-illuminated pixel collects a significant amount of long wavelength light due to diffraction effects for pixel widths below 4 μm.

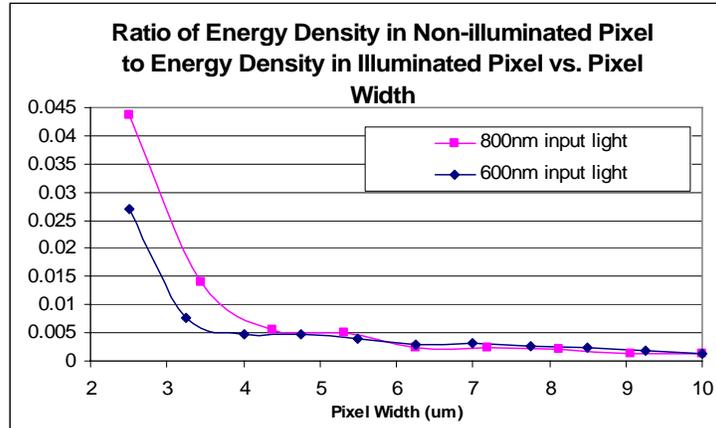


Figure 2: Energy density in non-illuminated pixel (to a depth of 3.5μm) vs. pixel width.

The second simulation measured the energy density as a function of depth beneath the metal wire (the collection region is shown in Figure 1), for a similar plane wave illumination. This profile (Single Metal Structure of Figure 3) provided information on the depth in silicon at which diffraction becomes considerable. The results in Figure 3 indicate that the majority of the absorption in the non-illuminated regions occurs at larger depths in the silicon, and therefore the diffraction effects could be significantly minimized by using shallower collection depths.

A second model placed a second set of metal wires 1 μm directly in front of the existing wires. A measurement of the energy density beneath the center of the metal as a function of depth into the silicon (Double Metal Structure of Figure 3) shows a significant decrease in the absorption at small depths.

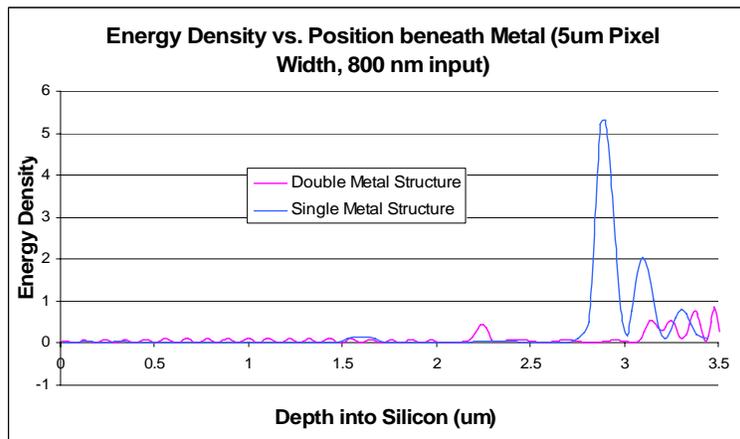


Figure 3: Energy density behind metal wires vs. depth into Silicon for the Single and Double Metal Structure.

The third simulation measured the energy density under the metal wire across a range of different pixel widths but also varied the vertical gap between the metal and the silicon surface (which was 1.5 μm in previous simulations). The results showed that the diffraction is reduced by moving to a vertical gap of less than 1 μm. Therefore, diffraction effects are minimized when the metal is closest to the surface of the silicon.

### 3. Summary

Degradation of resolution due to diffraction induced pixel cross talk becomes significant as the wavelength is increased or as the pixel size is decreased. This degradation can be reduced by decreasing the collection depth into the silicon, keeping the metal lines close to the silicon surface, or by adding an additional stack of metal lines.