An energy reduced sampling technique applied to a 10b 1MS/s SAR ADC

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***Abstract*—A 10-bit 1MS/s SAR ADC in 65nm CMOS is presented that introduces an Energy-Reduced-Sampling (ERS) technique to reduce the input drive energy for Nyquist rate ADCs. Our ADC occupies an area of 0.048 mm^2, and achieves an SFDR of 67 dB, an SNDR of 56 dB at up-to 1MS/s and 3.2µW power consumption, yielding a Walden Figure of Merit, FoM$_W$ of 5.9fJ/conversion-step. Using ERS, the peak sampling current and hence the input drive power is reduced by a factor 1.5 as compared to conventional sampling (CS). Considering an ideal Class A operation for the circuit driving the ADC, this translates into a minimum driver power consumption of 80µW for our ERS based ADC whereas it is 135µW for the conventional sampling, both much larger than the ADC power consumption of 3.2µW.**

Keywords— Nyquist sampling; input driver; SAR; adiabatic; SNDR; SFDR; Walden Figure-of-Merit

I. Introduction

Data acquisition systems targeted for low power wireless sensor nodes in IoTs, peripherals for microcontroller units (MCUs) emphasize on lowering the energy consumption of the standalone ADC. The Walden Figure-of-Merit, FoM$_W$ which has been used over the years to benchmark the standalone ADC performance seems to saturate near to 1fJ per conversion-step [1,2]. However, the energy consumption of the associated signal processing and the analog front end circuitry to drive the ADC inputs can be much higher than the ADC power consumption. More importantly, for these IoT applications, the analog front end driving the ADC has to be always ON in order to detect an event and present the signal to the ADC for conversion and further processing without significant latency or loss of critical information. Similarly in the case of analog peripherals for MCUs, the analog front end driver has to remain powered up so that the MCU based applications can continue to acquire data and convert whenever it is available whereas the digital peripherals can be switched off during the sleep modes. This calls for an equal if not greater attention to be paid to minimize the *input drive energy* of an ADC. The goal of this work is to present an Energy-Reduced-Sampling (ERS) based SAR ADC which helps to reduce the amount of energy required to drive the ADC inputs without degrading the ADC performance, so that the combined energy per conversion of driver plus the ADC is reduced.

II. Walden FoM vis-à-vis Input Drive Energy

To quantify the above argument, the minimum required input power to drive the corresponding ADC is computed for state-of-the-art FoM$_W$ SAR ADCs and compared with the ADC power consumption P_{ADC}. The minimum driver current (theoretical) required for slewing and linear settling, for near Nyquist rate sampling is $I_{DR,MIN} = N \cdot C_S \cdot (\Delta V_{MAX}/T_{TRACK})$. Here ΔV_{MAX} is the maximum signal change on the sampling capacitor C_S and N is the number of time constants (1 for slewing and SNR/9 for linear settling) required for ½ LSB settling at the end of tracking period T_{TRACK}; this T_{TRACK} is typically 10-20% of the clock period, $1/f_S$. As shown in Table 1, $I_{DR,MIN}$ is orders of magnitude more than the ADC supply current, I_{ADC} for the respective ADCs. For a driver operating at a supply voltage, V_{DD} and considering a track period of 10% of the clock cycle the minimum required input drive power $P_{IN,MIN} = 2 \cdot V_{DD} \cdot I_{DR,MIN}$ [5,6,8]. Assuming linear settling and that entire supply voltage V_{DD} is used for input signal swing (0-V_{PK}), for 100% driver efficiency, $P_{IN,MIN} > 10P_{ADC}$ for state-of-the-art FoM$_w$ ADCs, as shown in Table 1. Therefore, the actual bottleneck for low energy data acquisition systems lies in driving C_S which is not represented at all by FoM$_W$. This paper presents an energy-reduced-sampling (ERS) technique incorporated in a 10b charge redistribution SAR ADC, to reduce the ΔV_{MAX} and consequently reducing the input driver power without affecting the Dynamic Range (DR). Compared to CS, the ERS technique results in a lower input drive power P_{IN}, lower peak input currents thereby resulting in a lower energy consumption for the driver and ADC together.

III. Sampling technique and ADC Architecture

To demonstrate the concept of input drive power reduction, we designed a SAR ADC based on the work in [4], that can be configured for either ERS or CS as shown in Fig.1. Compared to [4], we implemented a pre-charge logic event-driven controller designed to operate at sampling rates ranging from 100kS/s up to 1MS/s at 1V supply. This allows for a wide sampling frequency range for the ADC, maintaining a constant FoM$_W$ for a fixed supply voltage. This ADC uses a split-capacitor DAC with a unit element of only 140aF and has the smallest reported DAC capacitance (145fF) for 10 bit accuracy for 1V input range. This is near to the minimum required DAC capacitance of 100fF according to kT/C limit.

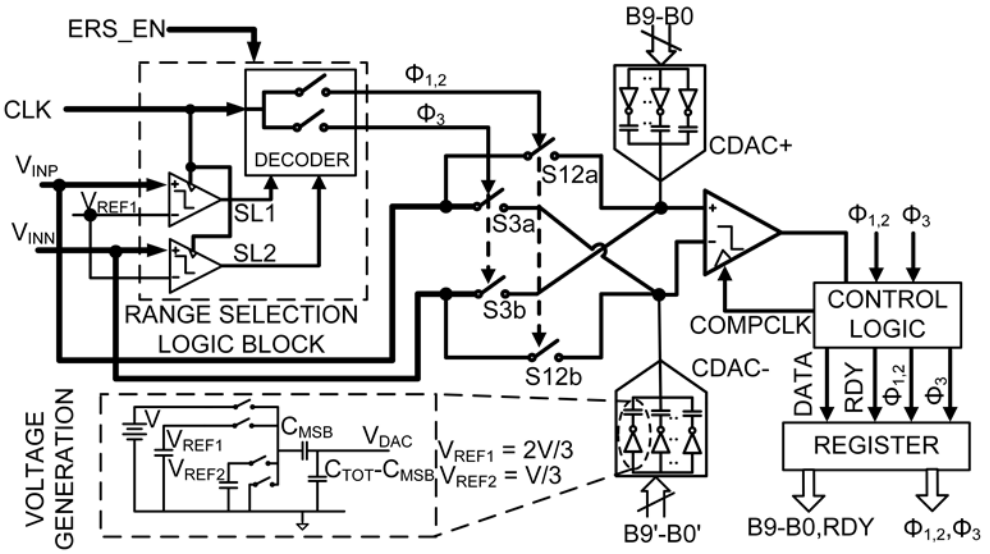

Fig. 1. Charge redistribution SAR ADC Architecture integrated with Energy-Reduced-Sampling technique.

Fig.2 shows the timing information together with the DAC voltages during an A/D conversion of near Nyquist rate inputs for both the ERS and CS. As shown for CS, maximum voltage change, ΔV_{CS} occurs at the sampling capacitor when sampling full-scale inputs, (0-V_{PK}) as V_{INP} and V_{INN} are always sampled onto C_{DAC+} and C_{DAC-} respectively. However for ERS technique, range-select (RS) block is enabled and it compares V_{INP} and V_{INN} to V_{REF1} (generated from the (dis)charging in the DAC array [4]) before sampling to determine the voltage range. Please note that although Fig.2 shows both V_{REF1} and V_{REF2} to define the three ranges, for differential inputs due to symmetricity, comparing (for example) V_{REF1} is sufficient for input range determination as shown in the RS block in Fig.1. Based on output of the RS block, either the signal $\Phi_{1,2}$ or Φ_3 enable the corresponding set of bootstrapped S/H switches, S12a/S12b or S3a/S3b respectively, as shown in Fig.1. In the presented ERS technique, three ranges are important; expressed in terms of V_{INP} and V_{INN}, these are :

Range 1: $V_{INP} > V_{REF1}$ and $V_{INN} < V_{REF1}$,
Range 2: $V_{INP}, V_{INN} < V_{REF1}$,
Range 3: $V_{INP} < V_{REF1}$ and $V_{INN} > V_{REF1}$.

Based on this range-select information, with ERS, C_{DAC+} samples V_{INP} for Range 1 and 2 and samples V_{INN} for Range 3, vice versa for C_{DAC-}. Therefore, (ideally) the maximum change that can occur across C_{DAC+} (C_{DAC-}) is $2V_{PK}/3$, which happens when V_{INP} (V_{INN}) changes from $V_{PK}(0)$ to V_{REF2} (V_{REF1}) at successive sampling instant. The frequency f_{IN} at which this maximum change $\Delta V_{MAX,ERS} = 2V_{PK}/3$ occurs for a sinusoidal input is close to $f_{IN} = 0.3 \cdot f_S$. This is in contrast to the maximum change of V_{PK} that occurs near $f_{IN} = 0.5 \cdot f_S$ for CS based ADCs. In terms of input sampling current requirement, this means that the peak input sampling current required for ERS is 1.5 times lower than that required for CS. Also the input frequency at which this maxima (peak) occurs is at a 1.7 times lower frequency than the near Nyquist input frequency, $0.5 \cdot f_S$, where traditionally the maxima (peak) of CS occurs. For near Nyquist rate

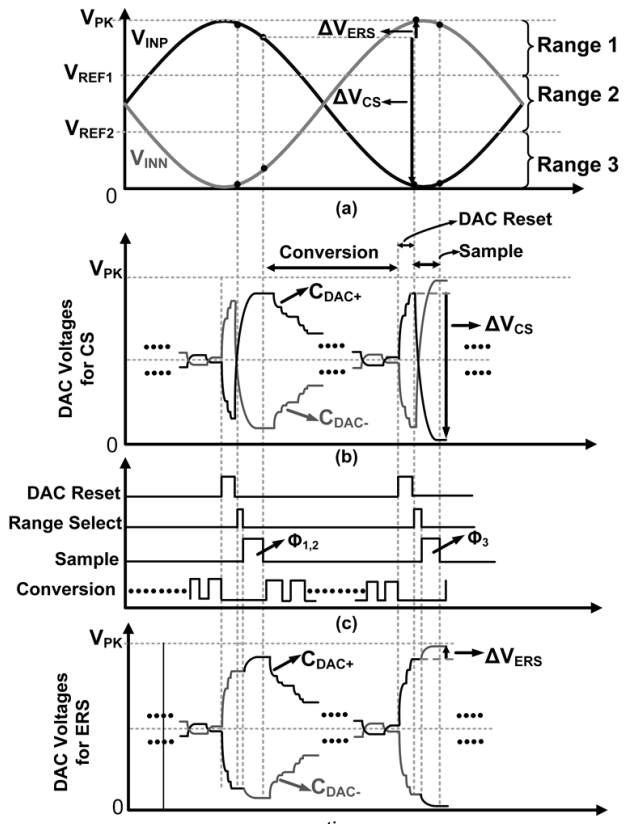

Fig. 2. (a) Input signals, V_{INP} & V_{INN} for near Nyquist rate sampling (b) DAC voltages for CS (c) Timing signals for ERS technique (d) DAC voltages for ERS based ADC highlighting the reduction in ΔV_{ERS}

inputs, when V_{INP} and V_{INN} alternate between range 1 and 3 at each successive sampling instant, the S/H switches S12a/S12b and S3a/S3b are enabled alternately by the RS block. This leads to C_{DAC+} alternately sampling V_{INP} and V_{INN}, and vice versa for C_{DAC-}, thereby resulting in an even smaller ΔV_{ERS} than ΔV_{CS}, as shown in Fig.2. When the inputs are in range 2, the RS block enables only S12a/S12b, the same as

in the CS mode. For near Nyquist operation, for the CS the maximum signal swing on C_{DAC+}/C_{DAC-}, $\Delta V_{MAX,CS} = V_{PK}$, whereas it is (ideally) $\Delta V_{ERS} = V_{PK}/3$ for ERS, while still presenting the FSR inputs to the ADC for conversion. This means for a near Nyquist rate operation, the peak input sampling current can be lowered by a factor of almost 3 for ERS in comparison to CS. For minimum power, the comparators in the RS block are scaled down in size compared to the ADC main comparator. Since the information from the RS block is only used to select the S/H switches, the accuracy of its comparators does not affect the final conversion accuracy. So even if the comparator's output in the RS block would be incorrect, the ADC output is still correct.

To measure the ADC's input sampling current profile, a measurement resistor, R_{MEAS} is placed in series with the input paths leading to the S/H switches. The maximum allowed input impedance for ½ LSB linear settling at the end of tracking period is, $N \cdot R_{IN,MAX} \cdot C \leq 1/(10 \cdot f_S)$. Also the input bandwidth $1/(2 \cdot \pi \cdot R_{IN,MAX} \cdot C_S)$ of the sampler should meet the ½ LSB tracking requirement for maximum rate of change of input. For the bootstrapped S/H switch resistance, R_{SW} of approximately 7kΩ in our ADC, R_{MEAS} is chosen as 1kΩ so that total input resistance $R_{IN} = (R_{MEAS}+R_{SW})$ is a factor 6 lower than the theoretical limit $R_{IN,MAX}$ of approximately 50 kΩ. This is done in order to settle with > 10-bit accuracy and to not limit the ADC linearity at the sampler. On-chip amplifiers measure the voltage across these resistors; their outputs are probed off-chip using a 20GHz sampling scope.

IV. Measurements and Results

Fig. 3 shows the die micrograph fabricated in a standard 65nm CMOS process with an active area of 0.048 mm².

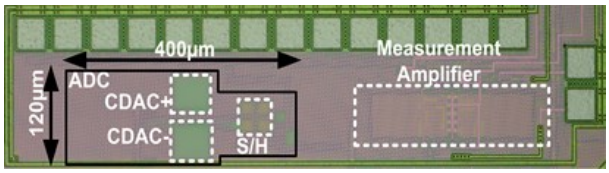

Fig. 3. Chip photograph

As evidenced by the sampling current profiles for ERS and CS in Fig.4 measured for near Nyquist rate sinusoidal input, the peak input current for ERS is reduced by a factor 2.3 for f_{IN} near to $f_S/2$. Note that the peak input current for the ERS based ADC occurs when sampling the inputs in range 2, and not in range 1 or 3 as for CS. Fig.5 shows the simulated peak input sampling current for both ERS and CS techniques along with measured data points as function of f_{IN} for sinusoidal inputs. Fig.5 shows that the peak sampling current for ERS occurs near $f_{IN} = 0.3 \cdot f_S$ in contrast to near $0.5 \cdot f_S$ for the CS. Even though it appears that the peak sampling current for ERS is higher for $f_{IN} < 0.3 \cdot f_S$, the overall peak for ERS over the entire input frequency range is still 1.5 times lower in comparison to CS. Noting that ADC drivers, specially source followers are usually designed to handle maximum drive (peak sampling)

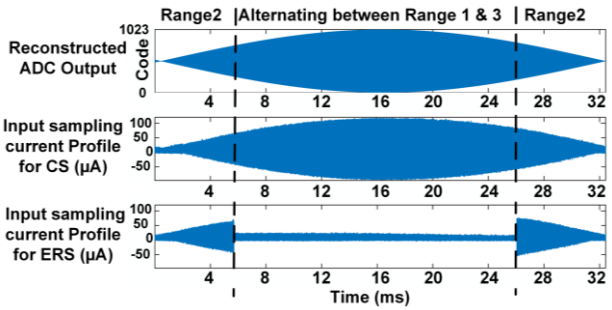

Fig. 4. Measured sampling current profile envelope at Fs–2*Fin, for both CS and ERS for Fin = 499.96875kHz and Fs = 1MHz.

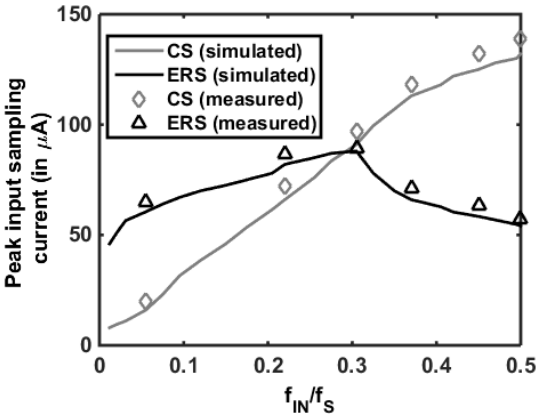

Fig. 5. Peak input sampling current of the ERS and CS based ADCs sampling current profiles as seen in Fig.4 for various input frequencies

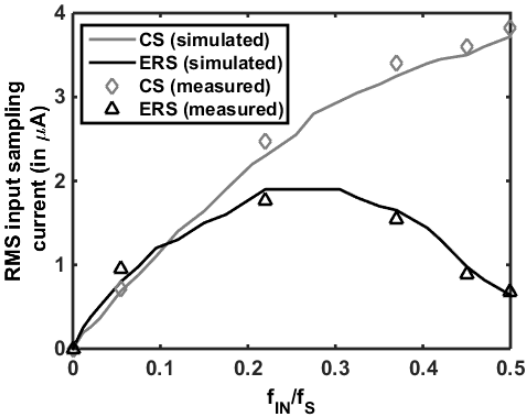

Fig. 6. RMS sampling current of the ERS and CS based ADCs sampling current profiles as seen in Fig.4 for various input frequencies.

currents to allow for initial slewing and linear settling, this implies that the drive power for a Class A input driver for the ADC, P_{IN} can be decreased by atleast a factor 1.5 using ERS. Using the expressions from Section II for an ideal Class A behavior, P_{IN} is found to be reduced from 135µW for CS to 80µW for ERS, for P_{ADC} of only 3 µW. This shows that the driver power is dominant over the ADC power consumption and hence the reduction in P_{IN} by a factor 1.5 for ERS technique is noteworthy. Fig.6 shows that for the sinusoidal input signals, the RMS value of the sampling current in the measured sampling current profile for the ERS based ADC is also less in comparison to the CS and is

approximately one-third of the latter for near Nyquist inputs. This shows that the ERS technique also helps in reducing the dynamic power consumption of the driver. Fig. 7 shows that the design achieves 67dB SFDR and 56dB SNDR with a 9.07 ENOB at a 1.7V peak-peak differential input using ERS. The dominant spur with ERS occurs at (f_S-2·f_{IN}), which originates from the mismatch of the ADC differential input channels. As shown in our measurements, this spur has negligible effect on the ADC's SNDR. Due to a smaller $\Delta V_{MAX,ERS}$ than $\Delta V_{MAX,CS}$ across the S/H switches, the body effect on its threshold voltage is decreased and hence their linearity is improved. This is evident from the 3dB improvement in SFDR (Fig.8) when using ERS. The ADC has +0.15/-0.95 LSB DNL and +0.4/-0.98 LSB INL for both ERS and CS based SAR ADC without calibration.

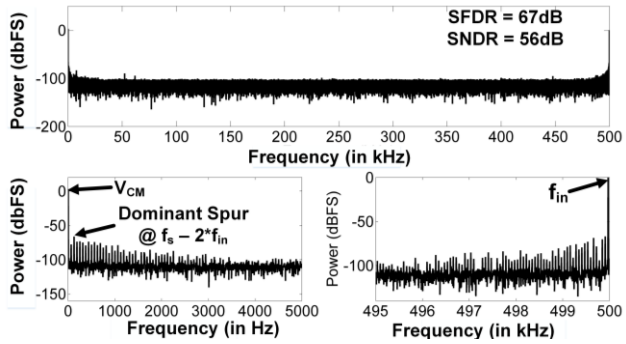

Fig. 7. FFT of the measured ERS based ADC output, normalized to the input tone Fin = 499.96875kHz and Fs = 1MHz.

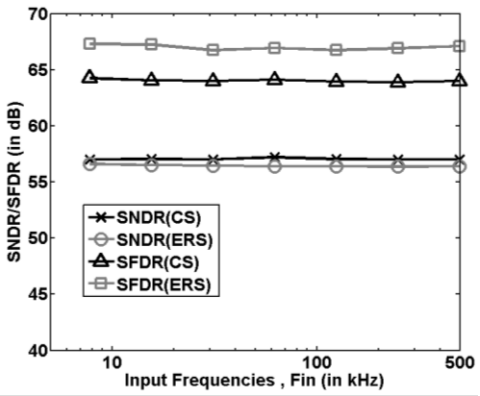

Fig. 8. Comparison of SNDR, SFDR for the ERS and CS based ADCs across input frequencies

Our ERS based ADC achieves a FoM_W of 5.9fJ/conversion over a sampling rate from 100kS/s to 1MS/s, comparable to state-of-the-art SAR ADCs offering such a wide range of sampling frequency [7,9]. Please note that there is no degradation in FoM_W due to the ERS technique in comparison to CS, thereby confirming that it does not degrade the SAR ADC performance. Also the ERS technique has no area penalty when applied to a SAR ADC. Table 1 compares the performance of the proposed ERS based SAR ADC to state-of-the-art FoM_W SAR ADCs. Please note that the measured power for both EMS and CS in our ADC is approximately a factor 6 more than the theoretical minimum which is due to the input impedance, R_{IN} chosen almost 6 times less than theoretical maximum to avoid limiting the linearity of the SAR ADC at the front end sampler for the wide span of sampling frequency range.

Table 1 : Comparison of ERS based ADC with state-of-art FoM_W ADCs

Architecture	This Work		[2]	[7]	[9]
	SAR with ERS	SAR with CS			
Technology	65nm	65nm	90nm	65nm	90nm
Resolution[bits]	10	10	11	10	10
Supply [V]	1	1	0.3	0.7	0.7
Maximum Sampling Rate	1 MS/s	1 MS/s	600 kS/s	2 MS/s	4 MS/s
Ideal Diff. Input Swing, V_{PK-PK} [V]	2	2	1.2	1.4	1.4
ADC Supply Current, I_{ADC} (µA)	3.2	3.2	0.62	4	15.7
$I_{DR,MIN}$ (µA), Theoretical input (driver) current	12	20	60	100	980
P_{ADC} (in µW)	3.2	3.2	0.2	3.6	11
$P_{IN,MIN}$ (in µW), Theoretical input (driver) power	12	20	36	70	600
P_{IN} (in µW), Measured input (driver) power	80	135	No data	No data	No data
ENOB [bits]	9.07	9.17	9.46	9.3	9.05
FoM_w (fJ/conversion)	5.9	5.5	0.44	2.8	5.2
Area (in mm^2)	0.048	0.048	0.035	0.047	0.042

V. Conclusion

An energy-reduced-sampling (ERS) technique to reduce the input driver power consumption for Nyquist rate ADCs has been demonstrated, which to the best of our knowledge is the first reported work to demonstrate on reduction of ADC's drive power requirement. The ERS based SAR ADC reduces the peak sampling current requirement by 1.5 times compared to CS, without degrading the ADC performance. Considering an ideal Class A behavior, the input power can be reduced from 135µW for conventional sampling to 80µW for the case of ERS in our ADC, while the ADC dissipates 3.2µW. Since the input driver power consumption as measured is order of magnitude greater than the ADC power, this reduction in input driver power by a factor 1.5 is significant in reducing the overall driver plus the ADC power dissipation. In addition the RMS value of the sampling current is also reduced by atleast a factor 3 which shows that the dynamic power consumption of the input driver can also be reduced through ERS.

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