A radiation-hardened µHz-range 24-bit 2.5-mW digital-to-analog converter

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ABSTRACT

We present a 24-bit sigma-delta charge-redistributing digital-to-analog converter (DAC). It is designed to have high absolute accuracy, low flicker noise and low power consumption, and is robust against temperature variations. The DAC was originally designed for space applications (a preliminary study for the ExoMars mission) and is radiation hardened by design. Its properties also make it ideally suited for other demanding control and calibration applications in a wide variety of environments.

The DAC uses a recursive second-order sigma-delta modulator, which combines high resolution with low out-of-band noise. Besides the modulator, the DAC also contains a dynamic element matching algorithm and a charge-redistributing front-end. Radiation hardening was already taken into account in the architecture phase and motivated the choice for a switched-capacitor DAC. This meant that the hardening of the analog circuit required only a small effort in the design and layout phase. For the digital part of the DAC, we use the DARE kit.

The DAC is designed for a thermal noise level of −144 dBV (0 – 50 Hz) and an out-of-band noise level of <−60 dB relative to full scale. It achieves a low-frequency noise level of −131 dBV (10 µHz – 1 Hz), and a gain stability vs. temperature of <2 ppm/K. It has a power consumption of 2.5 mW and an active area of 2.22 mm^2 in a 0.18 µm CMOS process with a MIM capacitor option. Total ionizing dose (TID) tests up to 133 krad showed no parameter shift in the DAC. Preliminary single event effects (SEE) tests with a Californium-252 source showed only one small transient at the DAC output in two tests lasting three days each.

INTRODUCTION

The DAC presented here was designed specifically for a seismic measurement system (SEIS) aboard the Humboldt payload that was part of ESA's upcoming 'ExoMars' mission. Unfortunately, the Humboldt payload was dropped by ESA due to financial constraints. In this application, the signal bandwidth is only 10 Hz or 50 Hz (depending on the mode of operation), but it extends down to 10 µHz, setting stringent limits on the tolerable amount of 1/f noise and drift over temperature. It is also required that the DAC is radiation tolerant by design, due to the high radiation levels encountered on its journey to Mars, and on Mars itself. To meet these requirements a special sigma-delta modulator was used with weighted outputs together with capacitors as DAC elements.

More generally, in many low-speed systems, such as process control, actuator/servo systems or gain and offset calibration, a high-accuracy DAC is required. Apart from high accuracy, these converters need to have low latency and low phase shifts when they are used inside a control loop, to keep the loop stable. Other common requirements are low offset, high absolute accuracy and low temperature dependence, especially if the converters are used for calibration purposes.

Sigma-delta converters seem ideally suitable for such applications as they can provide high resolution, while they need only limited analog component accuracy [1]. However, conventional sigma-delta modulators produce a lot of high-frequency quantization noise outside the signal band, due to the very limited number of quantization steps. An analog filter is therefore usually included in a sigma-delta converter to attenuate the quantization noise power. However, filtering with low corner frequencies will introduce phase-shifts that degrade the performance of the control system.

To circumvent these drawbacks, this paper presents a high-resolution sigma-delta DAC that has a low out-of-band noise (OOBN) power without using analog filtering, with low latency and no phase distortion.

A block diagram of the DAC is shown in Fig. 1. The DAC contains a sigma delta modulator, a dynamic element matching unit, and a charge-redistribution front-end. These are described in the sections below. Then, measurement results are presented and conclusions are drawn.

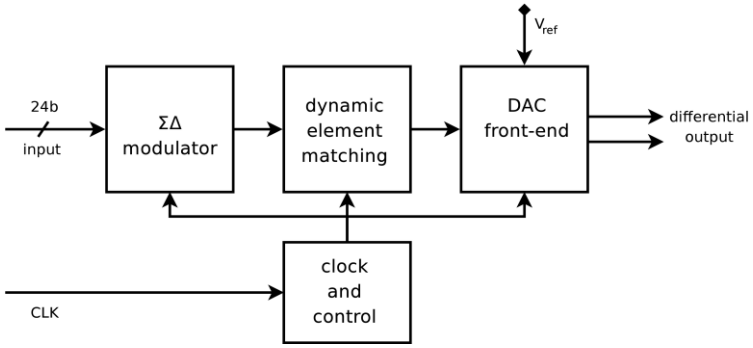

Fig. 1 DAC block diagram

SIGMA-DELTA MODULATOR AND DYNAMIC ELEMENT MATCHING

A recursive sigma-delta modulator combines high resolution with low out-of-band noise (OOBN) [2]. Low OOBN means that no or less analog lowpass filtering is necessary, which is important for low latency and low phase distortion. In Fig. 2, a schematic of such a recursive modulator is shown. As can be seen in the figure, the first modulator processes the signal, while the second modulator processes the quantization noise of the first to cancel it at the output. The third modulator cancels the noise of the second and so on. What is important is that, in contrary to other cascaded sigma-delta structures such as MASH [1], all modulators create noise-shaped signals and can simply be added together at the output without further processing. The noise-shaping of the individual signals guarantees that mismatch between the weights of the different stages does not immediately increase quantization noise.

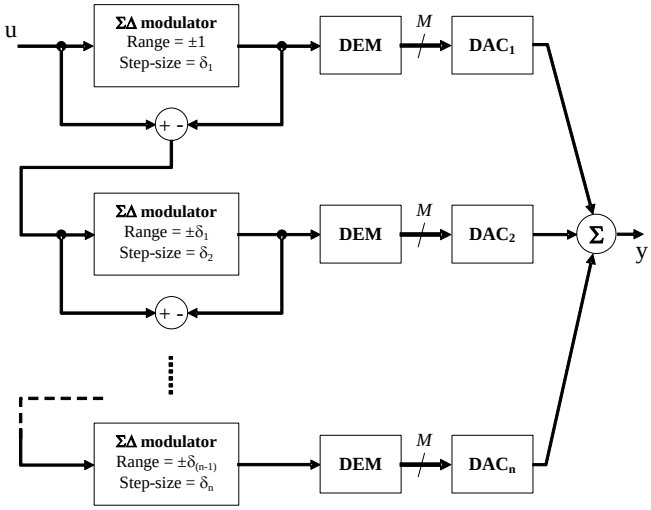

Fig. 2 recursive sigma-delta modulator

In this DAC implementation second-order loop filters are used for each stage, with five DAC elements per stage.

A dither circuit was added that supplies each stage with dither. A simple shift register is used to create a maximum-length sequence (MLS) and this bit sequence is used as dither. To ensure that the base period of the MLS is not located

inside the signal band, a 52-bit shift register is used. This creates a period of 4.5e15 samples, amounting to 2854 years when the generator and the modulator run at a rate of 50kHz.

To ensure robustness against mismatch within a stage, dynamic element matching (DEM) is used. We implement this with a standard data-weighted averaging (DWA) algorithm [3].

The design has only 4.25 μs delay between the load of a new input sample and the time it becomes available at the output of the DAC.

All digital blocks, including the modulator and the dynamic element matching unit, have been implemented using standard digital cells from a special radiation hardened design kit. This 'DARE' kit gives radiation hardening in the normal UMC 0.18μm CMOS process, using both circuit and layout techniques. [4].

CHARGE-REDISTRIBUTION FRONT-END

A charge redistribution front-end was chosen because capacitors are hardly sensitive to radiation, and because of its low 1/f noise. Furthermore, since the output voltage ultimately only depends on a ratio of capacitors, it will be largely independent of both temperature and process spread.

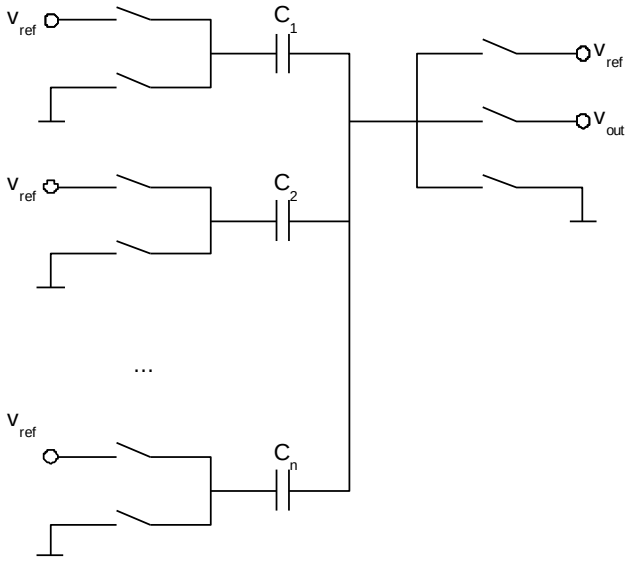

Fig. 3 DAC front-end schematic

A schematic of the charge redistribution front-end of the DAC is shown in Fig. 3. The switches are used to charge the capacitors corresponding to the DAC elements that should be turned on. The redistributed charge is then proportional to the wanted output voltage.

As stated above, capacitors are hardly sensitive to radiation. Furthermore, any parameter shift in the switches will hardly impact performance, as long as settling is still complete. This is easily achieved with some overdesign. Therefore, this type of front-end is very robust to total ionizing dose (TID). With respect to single event effects (SEE), the DAC capacitors are periodically reset, to avoid any long-lasting effects. Furthermore, all memory has been moved to the digital section that has been implemented using the DARE kit (see above). To prevent latch-up due to high-energetic particles (single-event latch-up, or SEL), guard rings have been placed around all transistors [5].

The DAC consists of 7 stages of 5 elements each. This results in 35 capacitors per single-ended halve of the differential DAC. The seven stages are scaled by a factor of three, from 1, 3, 9, 27, 81, 243 to 729 unit capacitors. This results in 5465 unit capacitors with a total capacitance of 200 pF per DAC halve. With a switching frequency of 1 MHz, this results in a differential output resistance of 10 kΩ, and a kT/C noise of −144 dBV from 0 – 50 Hz.

Due to the nature of a charge redistribution DAC, the output signal with all input bits '1', cannot exceed the reference voltage of 1.8V. As only the first stage of the recursive modulator is used for the signal, this limits the modulation depth of the converter to 63%. This leads to an output range of ±1.14 V, or 1.1 dBV.

MEASUREMENT RESULTS

The DAC has been fabricated in a 0.18 µm CMOS process with a MIM capacitor option. See Fig. 4 for a die photograph. The DAC output signal has been measured using both an ADC that is integrated on the test board (CS5534), and a HP3458A voltmeter.

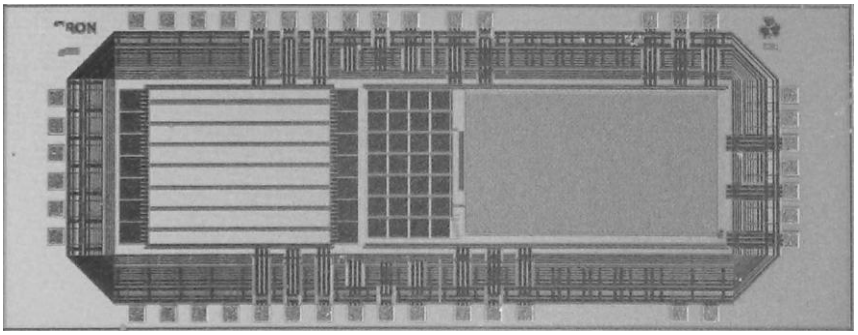

Fig. 4 Die photograph of the test chip. From left to right, the digital section, decoupling capacitors and DAC front-end capacitors can be seen.

In Fig. 5, the measured low-frequency output noise of the DAC can be seen, at an output voltage of 0 V. Over the shown frequency range of 10 µHz to 2 Hz, the noise follows a 1/f slope. The spurious tones seen above 30 mHz are due to the measurement setup. Due to the long integration time these spurious tones appear much stronger than the noise, but for tones one should look at the power level instead of the power density. With the axis on the right side of the graph, it can be seen that their levels are actually <−153 dBV, far smaller than 1 LSB.

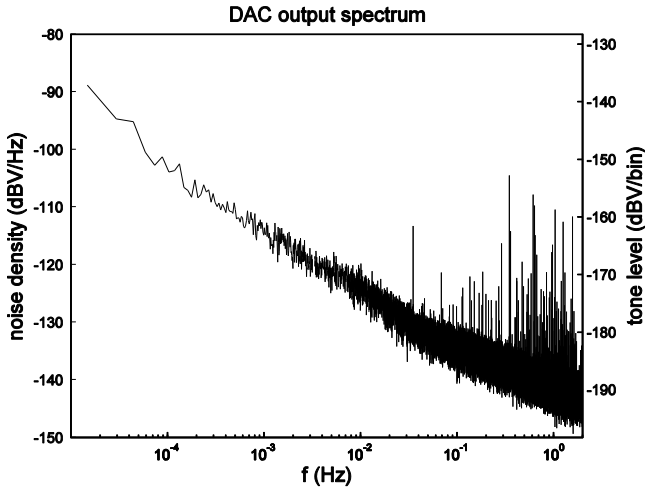

Fig. 5 measured noise spectrum at DAC output from 10 uHz – 2 Hz

Integrating the measured power spectrum over the frequency range from 10 µHz to 1 Hz yields a level of −131 dBV.

The measured output range of the DAC is ±1.08 V. This is about 6% lower than theoretically expected. This is due to the parasitic capacitance between the two complementary halves of the DAC. This parasitic capacitance can be lowered by a layout change, probably at the cost of reduced matching between the two DAC halves.

In Fig. 6, the measured DAC gain (with 1MΩ load resistance) can be seen as a function of temperature. In the worst-case range of −60 to −30 °C, gain variation is −1.5 ppm/K. This good result is obtained partly because two temperature effects in the DAC cancel each other. One is inherent to the DAC, and the other partly depends on the load. The worst-case gain instability is found with a very high load resistance, but is still low at 7 ppm/K. Improvements to the DAC are planned in order to make temperature behavior inherently robust, without relying on compensation.

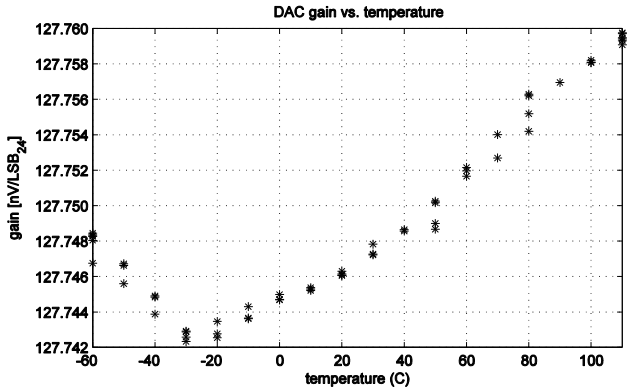

Fig. 6 measured DAC gain vs temperature

For linearity results, see Fig. 7. Here, the difference between the measured DAC output voltage (without load resistance) and an ideal linear transfer is shown. Distortion levels are −80 dB relative to full scale. This distortion is largely due to the non-linearity of the (MIM) DAC capacitors. This could be solved by dumping the charge of these DAC capacitors into the virtual ground input of a post-DAC opamp stage, eliminating any dependence on the linearity of the MIM capacitors. However, for the current application, these distortion levels are already more than adequate.

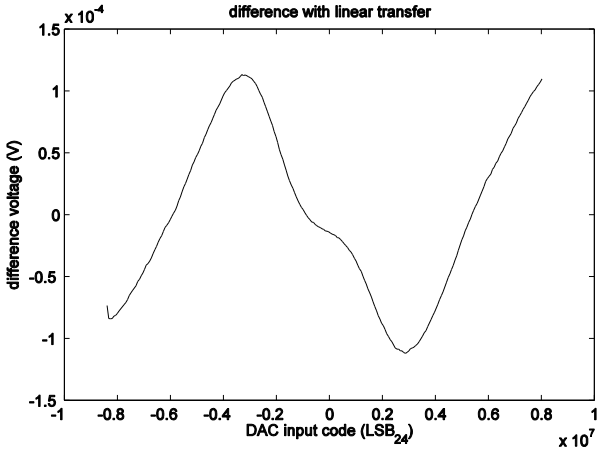

Fig. 7 difference between measured DAC output and ideal linear transfer

The measured output offset voltage has a mean value of −135 µV and a standard deviation of only 8 µV measured over 12 samples. The systematic part was unexpected, but with new layout extraction models, it matches simulation results. Chopping can be included in the design without much effort, and will remove this offset. Furthermore, chopping will reduce flicker noise even more.

Total ionizing dose tests have been performed up to 133 krad, using a Cobalt-60 source. No shift in DAC parameters has been observed. Up to 409 krad the devices are still fully functional but gave some deviations of the DAC parameters. Annealing and ageing reduces any offset and noise deviations induced by this larger dose rate back to zero.

Preliminary SEE tests using a Californium-252 source with an average linear energy transfer (LET) of 43 MeV/mg/cm^2 showed only one small transient at the output of the DAC in a test lasting several days. The power consumption of the

chip was also monitored by software, but no Single Event Latchups (SEL) were observed. Simulations were performed with SRIM to determine whether the neutron particles have sufficient penetration depth, but these show that the sensitive silicon depth is reached by the particles.

CONCLUSIONS

We have presented a high-resolution sigma-delta charge-redistribution DAC. It has low flicker noise, low power consumption and high stability with regard to radiation effects and temperature variation. It has a latency of only 4.25 μs and uses no internal filtering, which makes it very suitable for application inside control loops.

No shift in DAC parameters has been observed in TID tests up to 133 krad. Preliminary SEE tests using a Californium-252 source showed only one small transient at the output of the DAC in a test lasting several days.

The DAC achieves a noise level of −131 dBV in the band from 10 μHz to 1 Hz, and −60 dB out-of-band noise (OOBN). Its gain has a temperature dependence of <2 ppm/K. It consumes 2.5 mW and occupies an area of 2.22 mm^2. To the best of our knowledge, this is the best reported performance in this frequency range.

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