17.3 A Wideband Balun LNA I/Q-Mixer combination in 65nm CMOS

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Wideband receivers are required for many applications including the upcoming software-defined radio (SDR) architectures and ultra-wideband communication standards [1-3]. These standards cover a frequency spectrum from a few hundred MHz up to 6GHz. Co-operability with other communication devices (e.g., cellular and WLAN) operating in the same spectrum is mandatory, setting especially stringent demands on the wideband linearity of such receivers. The use of area-consuming on-chip inductors must be avoided as the cost per area of modern CMOS processes is high. The receiver preferably has a single-ended RF-input, as this avoids the use of an external broadband balun and its accompanying losses. A 65nm CMOS inductor-less wideband LNA-mixer topology is presented, merging a current commutating I/Q-mixer with a noise canceling balun-LNA.

Figure 17.3.1 shows the topology of the proposed receiver front-end, which combines the functionality of a balun, an LNA and an I/Q-Mixer (Blixer) into one circuit cell. The transistor in common-gate (CG) configuration gives wideband input matching ($Z_{in}\approx 1/g_m$). The inverter-based common-source (CS) stage produces a current in anti-phase with the CG output current, providing the single-to-differential conversion. The normally dominant thermal noise of the CG stage is canceled robustly [4]. The noise current of the CG transistor generates a noisy input voltage on the source resistance (R_S). This voltage results in an output current in the CS stage which is in-phase and fully correlated with the noise current of the CG transistor. The CG noise can thus be canceled at the differential output. The effective g_m of the CS stage is 4 times higher than the CG g_m in order to limit its noise contribution. The output currents of the CG and CS stage ($g_m \cdot v_{rf}$ and $4 \cdot g_m \cdot v_{rf}$ in Fig. 17.3.1) are distributed to two identical current-commutating mixer cells, as shown in Fig. 17.3.2. The drains of the transistors commutating the CS current are loaded by only ¼ of the total RC load. The difference in loading compensates the (4×) difference in g_m of the CG and CS stage, leading to equal conversion gain of the CG and CS side of the circuit. This gain balancing renders simultaneous canceling of the noise and distortion of the CG transistor, as in the LNA in [5]. However, in contrast to that design, here the canceling takes place at the IF output, after frequency translation. As the distortion of the CG transistor is canceled, the inverter-based CS stage is biased for minimal 2nd-order distortion to obtain a high IIP2 of the complete circuit. In contrast to narrowband systems 2nd-order distortion products can fall in-band, thus obtaining a high IIP2 is important for wideband receivers. The Blixer topology has only two internal RF nodes, the drains of the CG and CS transistors. The impedance at these points is set by the input impedance of the mixer devices. This impedance (~$1/g_m$ of the mixer transistors) is low, approximately 100Ω and 25Ω for the CG and CS side, respectively. The absence of high ohmic RF nodes makes wideband operation possible without requiring inductors.

Figure 17.3.3 shows the part of the circuit which is active when the local oscillator (LO) signal 'LO Q+' is high. The LO signal has a duty cycle of ¼, as shown in the lower right corner. At any moment in time, the CG and CS currents are switched to 1 of the 4 possible outputs. Consequently, the average current through the load is only ¼ of the sum of CG and CS output current. This allows for the use of relatively high resistors in the load, which result in a high gain, while the design still fits within a supply voltage of only 1.2V. In a stand-alone LNA, the capacitance at the load, due to parasitics and the next stage, will limit its wideband operation. In this combined LNA-mixer design, the capacitance at the load does not limit the RF bandwidth and is even required for correct operation. At the load, only the (low-frequency) IF signals are of interest. The capacitance at this node filters the IF output signal (1st-order filtering) and integrates the pulsed currents from the LNA part of the circuit.

The single-ended oscillator signal is generated externally. The on-chip LO-generation circuitry consists of a single-ended-to-differential converter, a divide-by-2 (I/Q-generator) and LO-buffers to drive the mixer core. A ¼ duty-cycle generator is implemented to generate the internal LO signals. The outputs of the mixer are buffered by means of source-followers ($R_{out}\approx 50\Omega$) which directly drive the output pads.

In [6] a mixer cell with single-ended input and differential output is presented. It uses a bipolar variant of the CG-CS input stage. In that design the possibility of noise canceling was not recognized nor used. Furthermore, two of these mixer-cells and an additional LNA would be needed for I/Q operation with acceptable NF. The merging of an LNA and I/Q-mixer is published in [7]. However, it is narrowband, uses 3 on-chip inductors and requires a differential RF-input signal. In contrast, this inductor-less design achieves wideband single-ended-to-differential operation and I/Q-mixing in one circuit cell.

The circuit is fabricated in a standard 65nm LP CMOS technology. A die micrograph and a detail of the PCB are shown in Fig. 17.3.7. The core measures less than 0.01mm^2. Measurements are performed on packaged PCB-mounted samples. The measured (voltage) conversion gain is 19dB with an IF bandwidth of 400MHz, as shown in Fig. 17.3.4. The DSB NF of the Blixer at a 3GHz LO frequency is around 4.5dB and flat over the IF bandwidth. The wideband RF performance is shown in Fig. 17.3.5. The gain remains flat within 1dB up to 7GHz. From 1 to 6GHz the NF is below 5dB, using a fixed IF of 50MHz. Note that this NF includes the PCB losses and that no balun is required. Above 7GHz the performance of the circuit generating the ¼ duty-cycle LO signals degrades and the gain and NF could not be determined. The S_{11} is below –10dB up to 7GHz. The wideband linearity is measured using a two tone test. The measured IIP3=–3dBm using two tones at 5.2 and 5.7GHz and a LO frequency of 4.6GHz. The IIP2=+20dBm, using 2.4GHz and 5.7GHz input tones and an LO of 3.2GHz. The intermodulation for tones that leak through the mixer is determined using a 5.7GHz and 5.8GHz signal. The product at 100MHz showed an IIP2>+40dBm, regardless of the LO frequency. The LO leakage to the RF input is below –60dBm for LO frequencies up to 4GHz and below –50dBm up to 7GHz. The quadrature phase and gain errors are below 3° and 1dB, respectively, measured on 2 packaged samples. The ¼-duty-cycle generation and LO buffers together consume 4-to-28mW for LO frequencies from 0.5 to 7GHz. Source-followers buffering the IF-outputs plus bias circuitry consume 13mW. The power consumption of the core circuit is 16mW from a 1.2V supply.

The achieved performance compares favorably to the state-of-the-art [1-3], especially with respect to RF bandwidth and linearity (see Fig. 17.3.6). The voltage conversion gain is high, considering that it is attained without an IF amplifier. The power consumption of circuit core is two times lower, and the active area is more than 4.5 times smaller than the reference designs.

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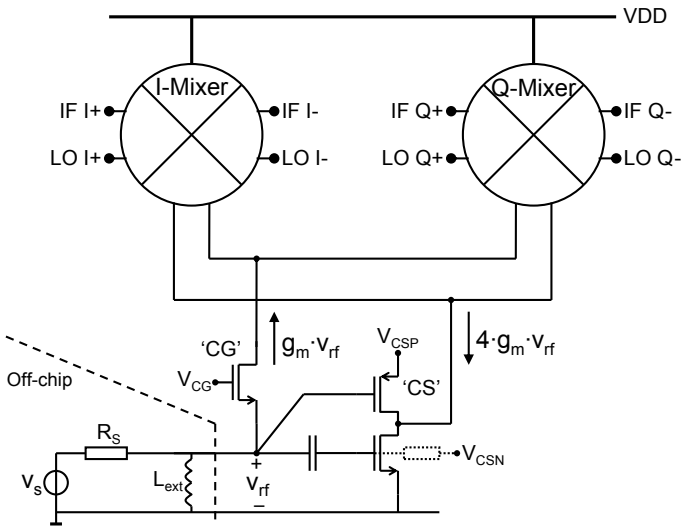

Figure 17.3.1: The Blixer, a stacked LNA-mixer topology with single-ended input and differential I/Q outputs.

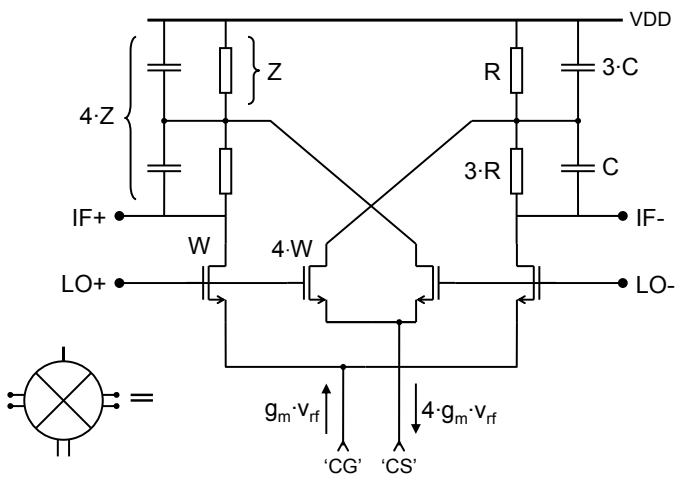

Figure 17.3.2: The mixer core.

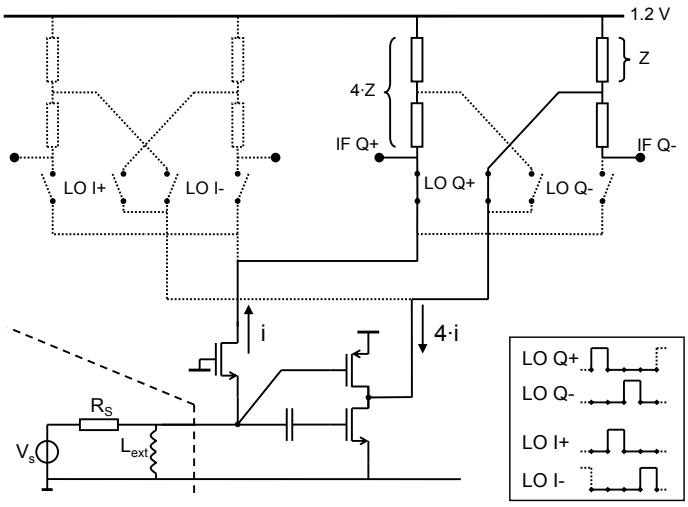

Figure 17.3.3: The active part of the circuit when LO Q+ is high.

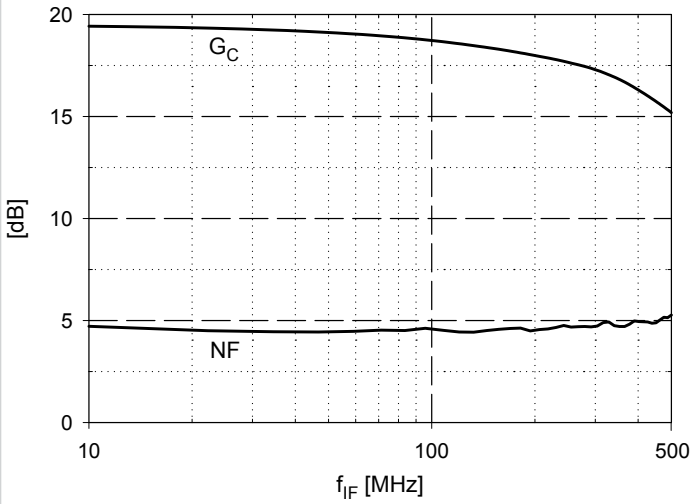

Figure 17.3.4: Conversion Gain (G_C) and NF for f_{LO}=3GHz.

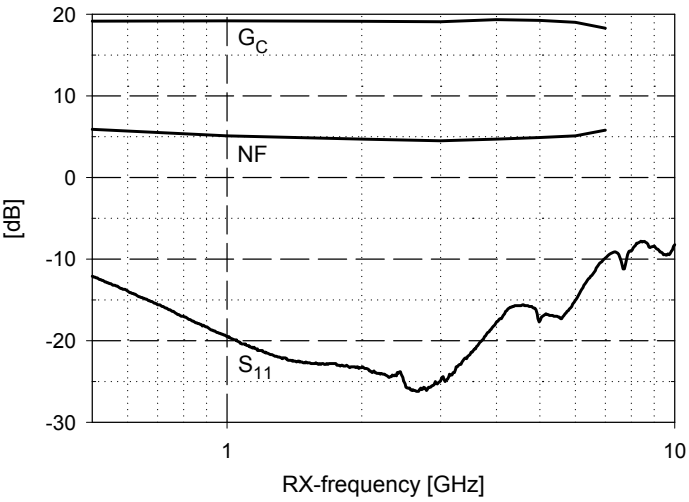

Figure 17.3.5: Conversion Gain (G_C), NF and S_{11} versus RX frequency (f_{IF}=50MHz).

Parameter		This Work	REF [1]	REF [2]	REF [3,8]
RX Frequency [GHz]		**0.5 – 7**	2 – 8	1.8 & 5 – 6	0.8 – 6
Gain [dB]		18 *excl.* IF-Amp	23 incl. IF-Amp	10 – 90 incl. IF-Amp	3 – 36 incl. IF-Amp
IIP3 [dB]		**-3**	-7	-9	-3.5
IIP2 @ RF [dB]		**+20**	+18	?	?
NF [dB]		5.5	4.5	4 – 8	5.5
S_{11} [dB]		-10	-8	-9	-10
Area* [mm²]	LNA + IQ-Mixers	**<0.01**	0.09	0.6	0.5
	LO Buffers (IQ)	**<0.01**		0.3	?
Power [mW]	LNA + IQ-Mixers	**16**	31	34 WLAN setting	29
	LO Buffers (IQ)	4 – 28	24	26 WLAN setting	?
CMOS Technology		65nm	65nm	0.13µm	90nm
VDD		1.2V	1.2V	1.2V	2.5V

* Estimated from chip micrographs

Figure 17.3.6: Comparison of wideband receive chains.

Continued on Page 617

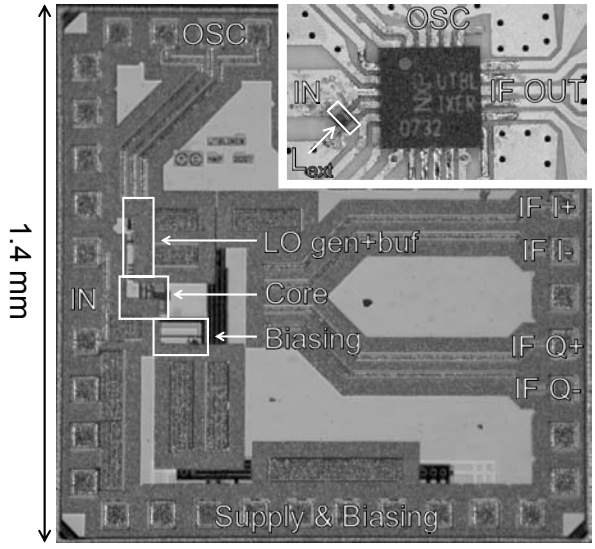

Figure 17.3.7: Chip micrograph and PCB detail showing a packaged sample.

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