

A Wide Tuning Range Voltage-Controlled Ring Oscillator dedicated to Ultrasound Transmitter

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Abstract: In this paper, a new design for a voltage-controlled ring oscillator (VCO) is presented. Implemented in 0.8 μm High-Voltage CMOS/DMOS technology provided by DALSA semiconductor with 5V power supply, this circuit uses relatively devices dimensions and low stages number to operate at low frequency. The new VCO combines three control methods to vary the oscillation frequency. The proposed VCO topology exhibits a very wide tuning range from 13 Hz to 407 MHz with good transient characteristics which is difficult to get from the conventional VCO. Its power consumption at the maximum oscillation frequency is 29.2 mW.

I. INTRODUCTION

A voltage-controlled oscillator (VCO) is considered as one of the important building blocks in analog and digital circuits. For example, in modern microcircuits, feeding clocks into chips must be avoided due to the effect of stray capacitance at the pins of IC package. High-speed circuits require on-chip oscillators to generate clocks. Besides of this, system synchronization needs to be realized by phase locked loop (PLL), which also has a VCO as a critical part. In recent years, LC oscillators [1] have been known with good phase noise performance, but their tuning range is relatively small (around 10-20%) and on-chip spiral inductors occupy a lot of chip area. On the other hand, ring oscillators usually have a wide tuning range, occupy less on-chip integration area, which makes them being more widely used than LC oscillators.

The design of a ring oscillator requires to connect odd number of inverters and feedback from the output of the last one to the input of the first one. Since the oscillation frequency is determined by the number of stages and the delay in each stage which is very small for an inverter, typically the achieved frequencies are several hundreds MHz to GHz in 0.8 μm technology. To achieve low frequency output, the number of stages has to be very large which is sometimes unacceptable. Many researches have been done to increase the delay for each stage instead of increasing the number of stages [2, 3, 4]. If the delay is voltage-controllable, then a VCO with variable-frequency output is obtained.

There are also other methods to realize VCOs, such as the one proposed in [5] which is based on a dual ring oscillator and allow to change the number of inverting stages with a control voltage. In [6] a VCO with even number of delay cells and quadrature-phase outputs is presented which has lower phase-noise. None of these implemented is suitable for low frequency applications.

The proposed voltage-controlled ring oscillator is dedicated, among other, to biomedical applications. Among these applications the ultrasound transmitter. It requires a wide and very low frequency clock generator, followed by a high voltage pulse generator, used to excite the ultrasonic transducer element. By carefully adjusting the size of devices and control voltages, the VCO shows out a very wide tuning range and good transient characteristics.

Section II presents the circuit implementation and design consideration of the proposed VCO. The simulation results are shown in section III, and conclusions are the subject of section IV.

II. DESIGN IMPLEMENTATION

A conventional VCO, as shown in figure 1, is realized by N stages of inverters (N is an odd number), with a control mechanism of the current passing through these inverters. Usually we use one PMOS transistor to control the upper side current and an NMOS transistor to control the lower side one.

Assume that the gate parasitic capacitances C_g of the NMOS and PMOS transistors are equal, the frequency of the oscillation can be found as

$$f_{osc} = \frac{1}{2N\tau} \quad (1)$$

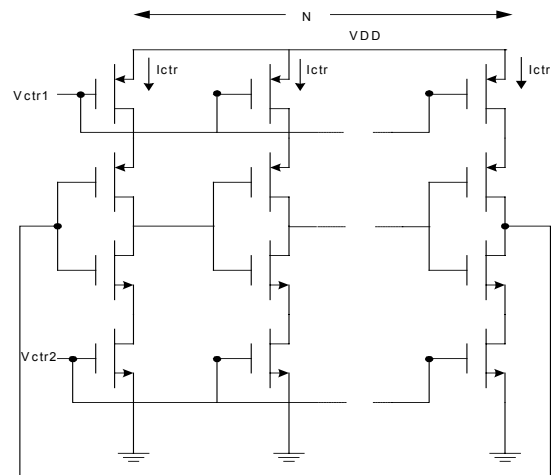


Fig. 1 Conventional VCO

where τ is the delay for one stage, which could be given by

$$\tau = \frac{V_{osc} C_g}{I_{ctrl}} \quad (2)$$

where V_{osc} is the oscillation amplitude, and I_{ctrl} is the control current. From the above two equations, we can get

$$f_{osc} = \frac{I_{ctrl}}{2N V_{osc} C_g} \quad (3)$$

It is obvious to see the oscillation frequency can be controlled by varying the control current, if assuming the number of stages N and C_g are fixed. The advantage for this configuration is that the oscillation frequency can be tuned for a wide range by changing the value of control current. However, when I_{ctrl} is very small, it is difficult to keep matching between its upper and lower limits. In addition, the small current will make the voltage swing slow and sometimes we will get a non-full swing signal at the output. Hence, good transient characteristic cannot be always obtained with this method.

In [3], the authors proposed a method to add controllable resistance at the input of each stage, thus increasing the delay, as shown in figure 2.

The delay τ of each stage can be calculated from figure 3, where g_m is the transconductance of each inverter and C_g is the parasitic capacitance of NMOS and PMOS transistors.

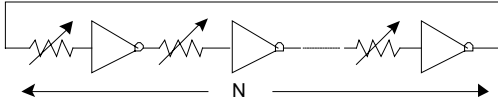


Fig. 2 VCO with controllable resistance

The delay τ of each stage can be approximated as follows:

$$\tau = \frac{C_g (1 + g_m R_V)}{g_m} \quad (4)$$

And the oscillation frequency is

$$f_{osc} = \frac{g_m}{2N C_g (1 + g_m R_V)} \quad (5)$$

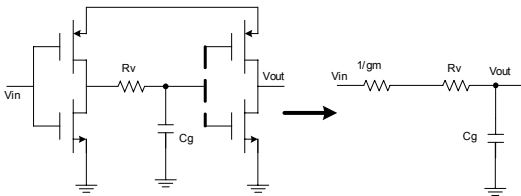


Fig. 3 Delay approximation for VCO with controllable resistance

From equation (5) we can see the oscillation frequency can be varied by changing the value of resistance R_V . Here C_g and g_m are assumed to be constant. Thus with large value R_V , low oscillation frequencies can be obtained using small size devices and less stages. The variable resistance can be realized with PMOS or NMOS transistors, as proposed in

[5]. However, using transmission gates enables a full swing between the power supplies. The resistance of a transmission gate can be controlled by its voltages V_p and V_n . Usually V_p equal to $V_{DD} - V_n$ for a symmetry reason.

Since the delay for each stage equals to the resistance of this stage multiplied by the capacitance of the input of the next stage, similar to the above method which changes the delay by adding controllable resistance, we can also get variable-frequency oscillator by adding controllable capacitance. Because the added capacitance C_C is in parallel with the parasitic capacitance C_g of the inverter, the delay for one stage becomes

$$\tau = \frac{C_g + C_C}{g_m} \quad (6)$$

and the oscillation frequency can be shown as

$$f_{osc} = \frac{g_m}{2N(C_g + C_C)} \quad (7)$$

The controllable capacitance can be realized by a dummy transistor with its bulk connected to ground and its source and drain connected to a control voltage (V_C), as shown in figure 4.

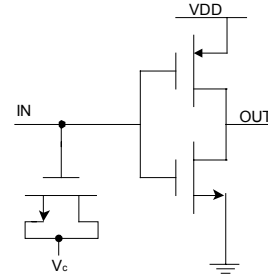


Fig. 4 One stage of VCO with controllable capacitance

From [7], the capacitance model of this dummy transistor can be shown as in Figure 5, where $V_{DS} = 0$ and $C_{gb} = WLC_{ox}$ in the worst case. When the gate voltage is much smaller than V_c , the other capacitances are relatively small compared with C_{gb} and when it is equal to V_c , the $C_{gb} = C_{ox}$ in series with the channel-to-bulk depletion capacitance and is considerably smaller. In this case, the relationship between the capacitance and the control voltage is complex and non-linear. However, when the control voltage equals to V_{DD} the minimum capacitance is given, where we can get maximum oscillation frequency. On the contrary, when it equals to V_{SS} and the gate-to-source voltage is higher than the transistor threshold voltage, the total capacitance of the transistor becomes $C_{gs} = WLC_{ox}$, which decreases the rising edge of the input signal and produces the minimum frequency.

This method is less widely used because the capacitance of the dummy transistors can not be changed sufficiently to get a wide range of the oscillation frequency. And for very low frequency VCO the size of the dummy transistors has to be very large to get large capacitance which occupies a

large area. However, if combined with other methods, it is still helpful to maximize the tuning frequency range.

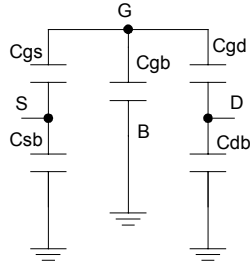


Fig. 5 Capacitance Model of a MOS transistor in its off state

The block diagram of the proposed VCO, is shown in figure 6. It is based on a 5-stage of delay cells (D1 to D5) connected on a loop and followed by a dividing circuit, and a set of inverters that act as the buffer (on a second driving stage) circuit. In order to obtain a wide tuning range, the conventional method is combined with the resistance-control method [2]. For the low oscillation frequency, a dummy transistor is added for each delay cell acting like controllable capacitance to further improve the tuning range.

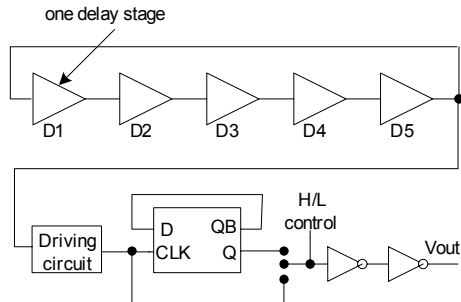


Fig. 6 Schematic for proposed VCO

Figure 7 shows one stage of the proposed VCO. It consists of one inverter with current controlled by a cascading NMOS transistor M1, one transmission gate as the controllable resistance and one dummy transistor as the controllable capacitance. By changing only one control voltage separately, the oscillation frequency can be varied according to equation (3), (5) and (7) respectively.

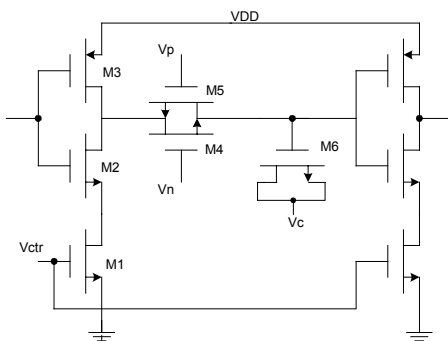


Fig. 7 Delay cell combining variable current, resistance and capacitance methods

As mentioned above, the disadvantage for the conventional VCO is that when the draining current is very small to get a low frequency oscillation, the signal swings slow and the circuit does not allow a full swing output. In other words, the transient characteristics tend to be not linear at low frequency. In order to avoid this problem, a divider by two is used at the output of the loop. It is based on a flip-flop with its inverting output feed back to its input, as shown in Figure 6. The flip-flop turns over each time when the front edge of the input arrives. Hence, it makes the output to be always 50% duty cycle regardless of the frequency. Also, it decreases the oscillating frequency by half period.

In the case of low frequency, the rising and falling times are relatively slow which avoid the divider to work properly. A driving circuit is used which consists of a set of inverters with their size being doubled one by one to increase their driving ability. The inverters after the flip-flop are used for the same purpose. Figure 8(a) shows the symmetric transient output wave after using divider, at frequency as low as 13 Hz, which is very difficult to get from other VCOs.

In the range of high frequency, however, the inverter always has enough current so we can get a symmetric output wave without using divider. Finally, an output multiplexer based on transmission gate and a control signal, used to control the tuning range by being with or without the divider. Table 1 gives the practical size for all transistors in each stage.

Table 1 : Practical size for transistors in delay cell

	M1	M2	M3	M4	M5	M6
W(μm)	12.8	1.6	3.2	2	4	1.6
L(μm)	1.6	0.8	0.8	0.8	0.8	0.8

III. SIMULATION RESULTS

The proposed VCO is implemented using $0.8\mu\text{m}$ CMOS/DMOS High-Voltage process technology provided by DALSA Semiconductor, with the size of transistors as shown in Table 1 and power supply equal to 5V. The simulation was done with Spectre under CADENCE platform.

Figure 8 shows the transient characteristics of the proposed VCO at frequencies of 13 Hz and 407 MHz respectively. The highest oscillation frequency was done with all the control voltages equal to VDD.

As mentioned above, the divider makes the output to be exactly 50% duty cycle at low frequency, whereas at high frequency the transient response is still good without the divider. Figure 9 shows the simulation result for output frequency versus control voltage characteristic of the proposed VCO. By fixing the control voltage for the resistance and capacitance switches and increasing the control voltage of the current through inverters, the frequency increased until 407 MHz. The curve for the control voltage of 1V to 1.8V, corresponding to the oscillation frequency of 70 MHz to 300 MHz, is almost

linear. By changing the other two control voltages, a different linearly control range can be obtained.

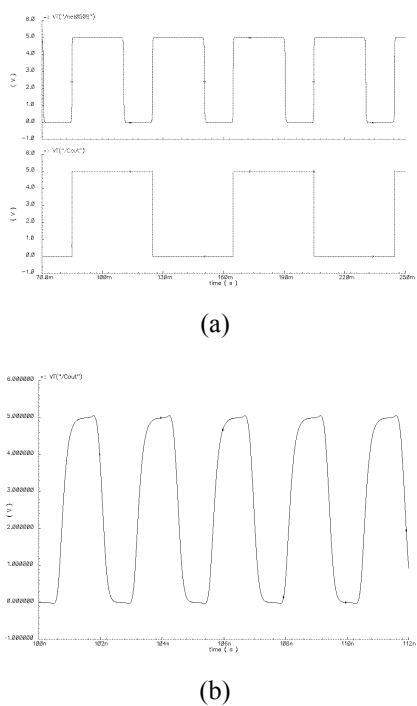


Fig. 8 Transient response of the VCO : (a) at frequency of 13 Hz With and without divider, (b) at frequency of 407 MHz

that when the control voltage increases, the oscillator runs faster, hence consumes more power. The maximum power dissipation that appears at highest frequency, is 29.2 mW. Figure 11 shows the sensitivity of VCO power supply. When the power supply is changed from 3 V to 5 V, the maximum frequency varies from 240 to 407 MHz.

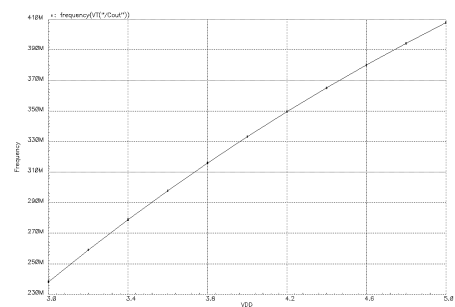


Fig. 11 Sensitivity of the VCO in function of the of the Power supply

IV. CONCLUSION

A new design for a voltage-controlled ring oscillator with wide tuning range from 13 Hz to 407 MHz has been presented. This topology combined the conventional VCO with resistance-control and capacitance-control methods together to maximize the tuning range. A divider is used to improve the transient characteristic at low frequency. Simulation results show the proposed VCO exhibits wide tuning range and good transient characteristics both at low and high frequencies.

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REFERENCES

- [1] Graninckx and Steyaert, M. "A 1.8-GHz Low-phase noise CMOS VCO using optimized hollow spiral inductors", IEEE J. Solid-State Circuits, Volume : 32, pp 736-744, May 1997.
- [2] Banu M., "100 khz – 1 ghz Nmos Variable-frequency Oscillator With Analog and Digital control", ISSCC, Solid-State Circuits Conference. Digest of Technical Papers. vol. 31, pp 20-21, Feb. 1998.
- [3] Retdian, N., Takagi, S. and Fujii, N., "Voltage controlled ring oscillator with wide tuning range and fast voltage swing", IEEE Asia-Pacific Conference, ASIC on 2002. Proceedings, pp 201 – 204, Aug. 2002.
- [4] Chen, O.T.-C., Sheen, R.R.-B., "A power-efficient wide-range phase-locked loop", IEEE Journal of Solid-State Circuits, Volume : 37, Issue: 1, pp 51 – 62, Jan. 2002.
- [5] Enam, S.K., Abidi, A. A., "A 300-MHz CMOS voltage-controlled ring oscillator", IEEE Journal of Solid-State Circuits, Volume: 25, Issue : 1, pp 312 – 315, Feb. 1990.
- [6] Sun L., Kwasniewski, T., and Iniewski, K., "A quadrature output voltage controlled ring oscillator based on three-stage sub-feedback loops", IEEE International Symposium on Circuits and Systems, 1999, Volume : 2, pp 176 – 179, May 1999.
- [7] Johns, D. and Martin, K., "Analog Integrated Circuit Design" John Wiley and Sons, New York, 1997.

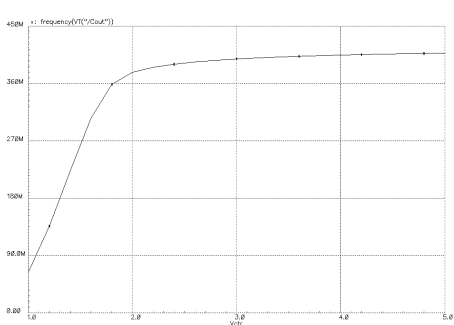


Fig. 9 Frequency versus control voltage

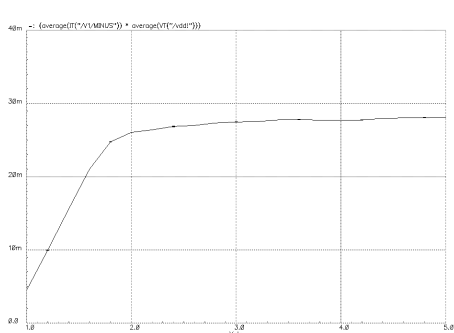


Fig. 10 Power dissipation versus control voltage

Another curve, presenting the power dissipation versus control voltage, is shown in figure 10. It is obvious to note