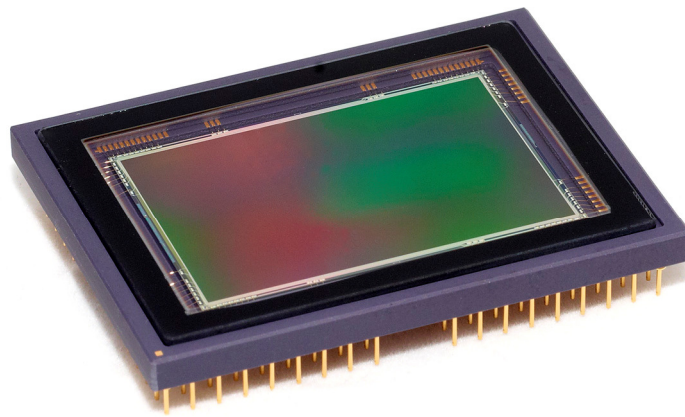


DATASHEET



FTF7046M

32M Full-Frame CCD Image Sensor

Product Specification

September 2013

TELEDYNE DALSA
Professional Imaging



32M Full-Frame CCD Image Sensor

FTF7046M

- Image format 36 x 24 mm²
- 32M active pixels (6936H x 4616V)
- Excellent anti-blooming and Variable electronic shuttering
- Square pixel structure (5.2 μm x 5.2 μm)
- Micro lenses with wide angular response
- >90% fill factor with micro-lenses
- High dynamic range (typ. 74 dB) and linear dynamic range (>72 dB)
- High sensitivity
- Perfectly matched to visual spectrum
- Low dark current and low fixed pattern noise
- Four readout registers with 1 low-noise amplifier per register, data rate up to 25MHz per output
- RoHS compliant

Description

The FTF7046M is a full-frame monochrome CCD image sensor with a 3:2 aspect ratio utilizing 6936 x 4616 active pixels of 5.2x5.2 μm². The active image area dimension is 36.067 x 24.003 mm².

The CCD has a very low dark current and a linear dynamic range of over 11 true bits at 60°C and 25 MHz readout frequency.

High quantum efficiency is achieved by using transparent membrane poly-silicon electrodes and micro-lenses.

The pixels have a vertical anti-blooming concept for excellent highlight handling and fast electronic shutter.

The device has four read-out registers, two at the bottom and two at the top. Four identical low-noise output amplifiers are located at opposite sides of the dual readout registers, for the registers closest to the image area the amplifier is located at the left side. This allows simultaneous readout out through one or two outputs, either at the bottom or at the top.

Sensors are produced in Teledyne DALSA's Advanced Technology (AT) in the Teledyne DALSA Semiconductor factory in Bromont, Canada.

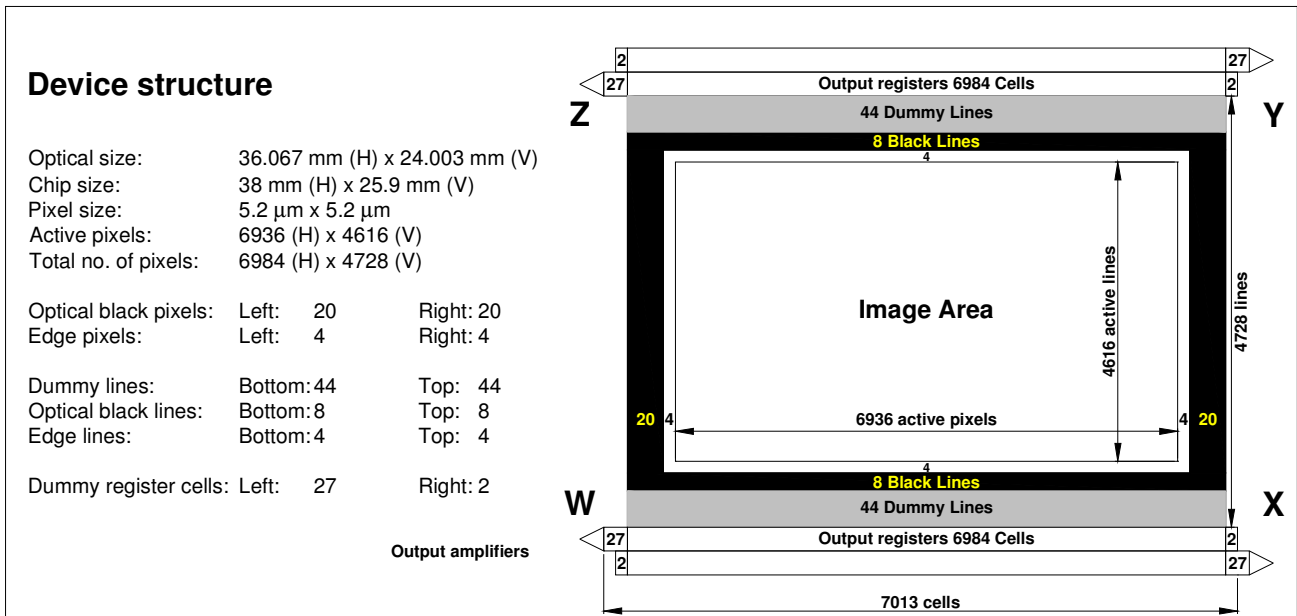


Figure 1: Device structure

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Architecture of the FTF7046M

The optical centers of all pixels in the image section form a square grid. The charge is generated and integrated in this section by setting two gates of the four-phase pixel (A1...A4) at the high integration voltage, and the other two gates at the low voltage. A separate transfer gate TG1 between the image section and output registers will enable sub-sampling features.

For readout, dual output registers are located below and above the image section. A transfer gate TG2 separates the two sections of the dual output registers. After the integration time, the image charge is shifted to either the upper or lower registers, one or two lines at a time, depending on the readout mode. This enables either

single or multiple read-outs. During vertical transport, the C3 gates separate the pixels in the registers. Each register is terminated by a separate summing gate and output gate.

The charge-to-voltage conversion is performed by a three-stage source follower amplifier (4 in total). The charge-to-voltage conversion node is reset to reset drain voltage (RD) by pulsing the reset gate (RG). The amplifier power supply is SFD, the ground terminal is SFS.

VNS and VPS are the bias voltages for the n-type substrate and for the CCD p-well, respectively.

IMAGE SECTION	
Image diagonal (active video only)	43.3 mm
Aspect ratio	3:2
Active image width x height	36.067 x 24.003 mm ²
Pixel width x height	5.2 x 5.2 μm ²
Fill factor	
with micro-lenses	>90%
Image clock pins	16 (4x4) pins (A1...A4)
Capacitance of each clock phase	100 nF per phase
Image Transfer Gates	2 pins each top and bottom (TG1)
Capacitance of each TG1	50 pF
Total number of lines	4728
Number of active lines	4616
Number of edge lines	8 (=2x4)
Number of black lines	16 (=2x8)
Number of dummy lines	88 (=2x44)
Total number of pixels per line	6984
Number of active pixels per line	6936
Number of edge (timing) pixels per line	8 (2x4)
Number of black reference pixels per line	40 (2x20)

OUTPUT REGISTERS	
Number of registers	4 (2 top / 2 bottom)
Total number of register cells per register	7013
Number of register cells below/above image	6984
Number of dummy register cells	29 (27 at output side, 2 at opposite side)
Output register horizontal transport clock pins	6 pins per dual register (C1T...C3T, C1B...C3B)
Capacitance of each C-clock phase	140 pF per pin/phase
Overlap capacitance between neighboring C-clocks	40 pF
Output register Transfer Gates	2 pins per dual register (TG2)
Capacitance of each TG2	50 pF
Output register Summing Gates	1 pin per output (SG)
Capacitance of each SG	15 pF
Reset Gate clock phases	1 pin per output (RG)
Capacitance of each RG	15 pF
Number of output buffers	4 (1 on each register)
Output buffer type	Three-stage source follower

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Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS¹	MIN	MAX	UNIT
GENERAL:			
storage temperature	-40	+80	°C
ambient temperature during operation	-20	+60	°C
voltage between any two gates	-20	+20	V
DC current through any clock phase (absolute value)	-0.2	+0.2	µA
OUT current (no short circuit protection)	0	+10	mA
VOLTAGES IN RELATION TO VPS:			
VNS, SFD, RD	-0.5	+30	V
SFS	-8	+5	V
All other pins	-20	+25	V
VOLTAGES IN RELATION TO VNS:			
SFD, RD	-15	+0.5	V
SFS, VPS	-30	+0.5	V
All other pins	-30	+0.5	V
VOLTAGES IN RELATION TO SFD:			
RD	-5	0	V
RG voltage	0	+30	V

¹ During Charge reset it is allowed to exceed maximum rating levels in relation to VNS, according to the specified DC voltage settings (see below) and AC clock level conditions (see next page).

Note on Voltage Settings

Since the AC signals for operating the horizontal register (register clocks C1T-C2T-C3T-C1B-C2B-C3B, summing gate SG) and the output stage (reset gate RG) are analog signals for the CCD, the optimal voltage settings can be influenced by the waveforms of these signals, which in turn depend on the layout and schematics of the camera electronics. Thus the optimal value of all DC biases mentioned can deviate up to +/-1V from the 'typical' values mentioned in the data sheets depending on the precise implementation of the hardware around the sensor. All DC and AC voltages settings in the following tables are measured on sensor pins.

DC Voltage Settings

DC CONDITIONS^{1,2}		MIN [V]	TYPICAL [V]	MAX [V]	MAX [mA]
VNS ³	n substrate	20	adjustable	28	15
VPS	p well	5.5	6	6.5	15
SFD ⁴	Source Follower Drain	19.5	20	20.5	4.5
SFS ⁴	Source Follower Source	0	0	0	1
VCS	Current Source	0	0	0	–
OG	Output Gate	5.0	6.0	8.0	–
RD	Reset Drain	19.5	20	20.5	–

¹ All voltages in relation to SFS; typical values are according to test conditions.

² Power-up sequence: VNS, SFD, RD, VPS, all others. The difference between SFD and RD should not exceed 5V during power up or down.

³ To set the VNS voltage for optimal vertical anti-blooming (VAB), it should be adjustable between minimum and maximum values.

⁴ Maximum current for each amplifier.

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AC Clock Settings

Following table shows the AC operating conditions.

AC CLOCK LEVEL CONDITIONS ¹	MIN	TYPICAL	MAX	UNIT
IMAGE CLOCKS (A)/ TRANSFER GATES 1 (TG1) ²				
A-clock amplitude during integration and hold (integration with 2 gates high)	10	11	11	V
A-clock amplitude during vertical transport (duty cycle=5/8) ³	12	13	14	V
A-clock low level	-	0	-	V
Charge Reset (CR) level on A-clock ⁴	-	0	-	V
OUTPUT REGISTER CLOCKS (C):				
C-clock amplitude (duty cycle during hor. transport=3/6)	4.75	5.0	5.5	V
C-clock low level	2.25	2.75	3.25	V
Summing Gate (SG) amplitude	4.75	5.0	5.5	V
Summing Gate (SG) low level	3.5	4.25	5.0	V
OTHER CLOCKS:				
Transfer Gate 2 ⁵ (TG2) amplitude during vertical transport	9	11	12	V
TG2 low level	-	0	-	V
Reset Gate (RG) amplitude	5	5	10	V
Reset Gate (RG) low level	-	17	-	V
Charge Reset (CR) pulse on Nsub ⁴	0	5	5	V

¹ All voltages in relation to SFS; typical values are according to test conditions

² Transfer Gate 1 should be clocked as A1 during normal transport or held low during a line shift to sub-sample image

³ Three-level clock is preferred for maximum charge

A two level clock can be used if a lower maximum charge handling capacity is allowed

⁴ Charge Reset is achieved by applying the CR Reset pulse on VNS while the A-clocks are set to the typical A-clock low level.

⁵ Transfer Gate 2 separates the two parallel output registers

AC CLOCK CHARACTERISTICS	MIN	TYPICAL	MAX	UNIT
Horizontal frequency (1/Tp) ¹	-	25	25	MHz
Vertical frequency ²	-	50	50	kHz
Charge Reset (CR) time	10	Line time	-	µs
Rise and fall times: image clocks (A), (TG)	10	20	-	ns
register clocks (C) ³	3	5	1/8 Tp	ns
summing gate (SG)	3	5	1/8 Tp	ns
reset gate (RG)	-	3	1/8 Tp	ns

¹ Tp = 1 clock period

² Higher frequency will limit Qmax and/or degrade charge transport efficiency

³ Duty cycle = 3/6

AC CLOCKING SEQUENCES	CHARGE TRANSFER DIRECTION
Vertical transport Image, to WX output register	A1 → A2 → A3 → A4
Vertical transport Image, to YZ output register	A1 → A4 → A3 → A2
Horizontal transport, top register (to W or Z output)	C1T → C2T → C3T
Horizontal transport, bottom register (to X or Y output)	C1B → C2B → C3B

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Performance

The following table shows the most important indicators that describe the performance of the device. A number of items are derived from measured parameter values, such as Dynamic Range and output voltage.

The test conditions for the performance characteristics are as follows:

- All values are measured using typical operating conditions.
- VNS is adjusted as low as possible while maintaining proper vertical anti-blooming
- Sensor temperature = 60 °C
- Horizontal transport frequency = 25MHz
- Vertical transport frequency = 50kHz
- Integration time = 100ms
- Linear Operation, Linear/Saturation and Dark Condition parameters are measured at W and X output.

PERFORMANCE	MIN	TYPICAL	MAX	UNIT
Qmax (full well capacity) ¹ in full-resolution mode	42000	45000		el
Qlin ² in full-resolution mode	37000	40000		el
Vout (at full well capacity)	1200	1485		mV
Conversion factor	31	33	35	μV/el
Mutual conversion factor mismatch (Δ ACF) ⁴		0	5	μV/el
Amplifier noise over full bandwidth after CDS		11	12	el
Dynamic Range (at 25 MHz) ⁵	70.9	72		dB
Linear Dynamic Range (at 25 MHz)	69.8	71		dB
Overexposure handling ³		200		x Qmax
Vertical Charge Transfer Efficiency ⁶	0.999 995	-	-	-
Horizontal Charge Transfer Efficiency ⁶	0.999 999	-	-	-
Image lag	-	0	0	%
Resolution (MTF) @96 lp/mm	55	-	-	%
Quantum Efficiency:				
Red (590nm)		30		%
Green (530nm)		37		%
Blue (480nm)		30		%
Sensitivity: @3200K, IR filter ⁷		80		el/lux.s
Block-to-block difference ⁸		1.0	3.0	%
Stitching effect ⁹		1.0	3.0	%
Low Pass Shading ¹⁰		2	5	%
Random Non-Uniformity (RNU) ¹¹		1	2	%

¹Qmax is determined from the low-pass filtered image

²The linear full-well capacity Qlin is calculated from linearity test. The test guarantees 97% linearity.

³Overexposure over entire area while maintaining good Vertical Anti-Blooming (VAB) is tested by measuring the dark line along the image section.

⁴Mismatch of the outputs is specified as Δ ACF with respect to reference measured at the operating point ($Q_{lin}/2$)

⁵Minimum Dynamic range is calculated with Min Qmax and Max Noise values

⁶Charge Transfer Efficiency values are tested by evaluation and expressed as the value per gate transfer

⁷Sensitivity is measured using illumination with a light source of 3200K color temperature and a CM500, 1mm thick IR filter

⁸Block-to-block difference is defined as the difference in average signal between different stitching blocks under illumination

⁹Stitching effect is defined the deviation of response under illumination of the lines or rows at the stitch lines compared to the average response

¹⁰Low Pass Shading is defined as the ratio of the one- σ value of an 8x8 pixel blurred image (low-pass) to the mean signal value

¹¹RNU is defined as the ratio of the one- σ value of the high-pass image to the mean signal of nominal light

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OUTPUT BUFFERS	MIN	TYPICAL	MAX	UNIT
Supply current	-	5	-	mA
Bandwidth ($R_{load}=3.3\text{ k}\Omega$)	100	130	-	MHz
Output impedance buffer ($R_{load}=3.3\text{ k}\Omega$, $C_{load}=2\text{ pF}$)	-	250	-	Ω

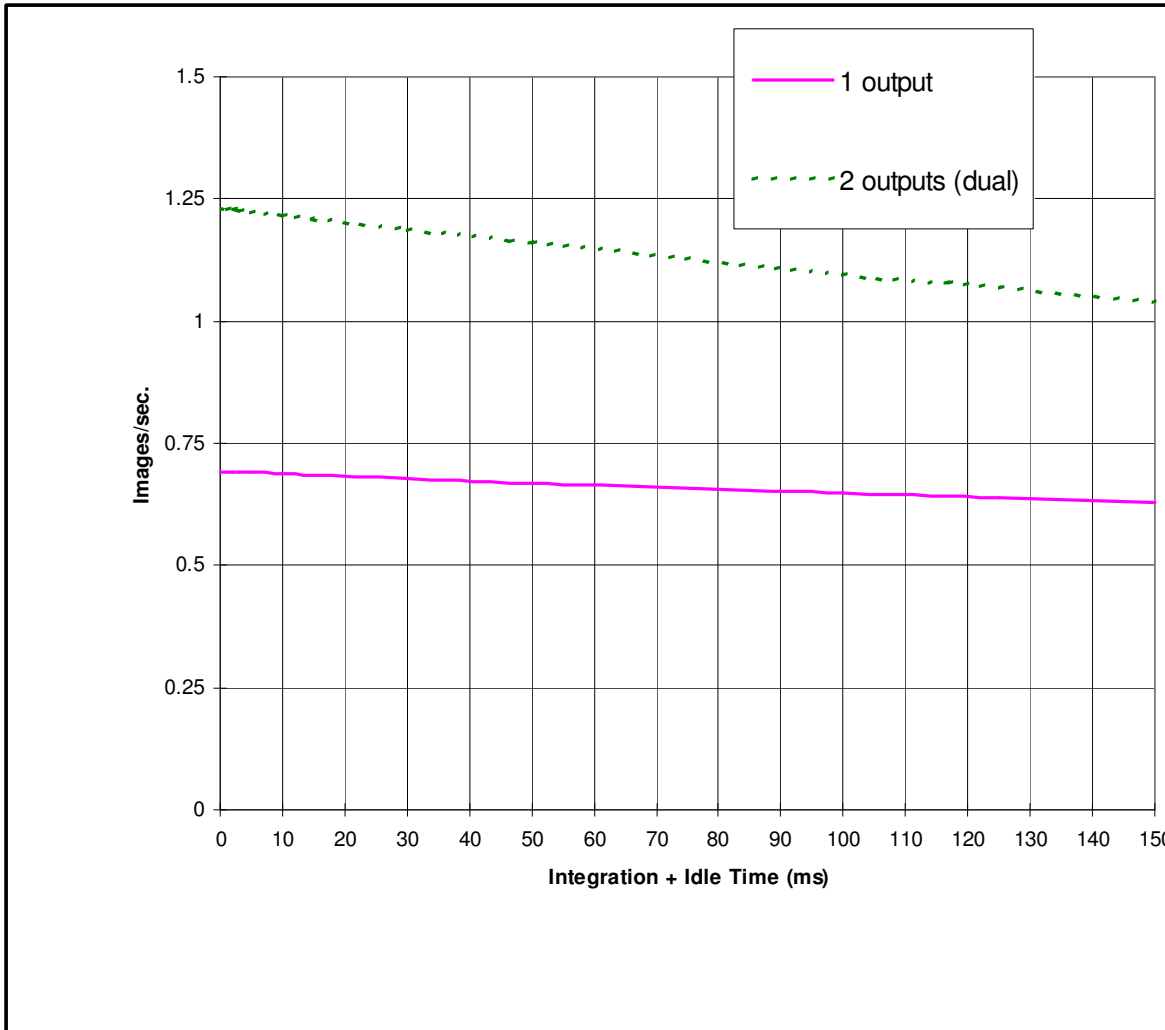


Figure 2: Maximum number of images/second versus integration time

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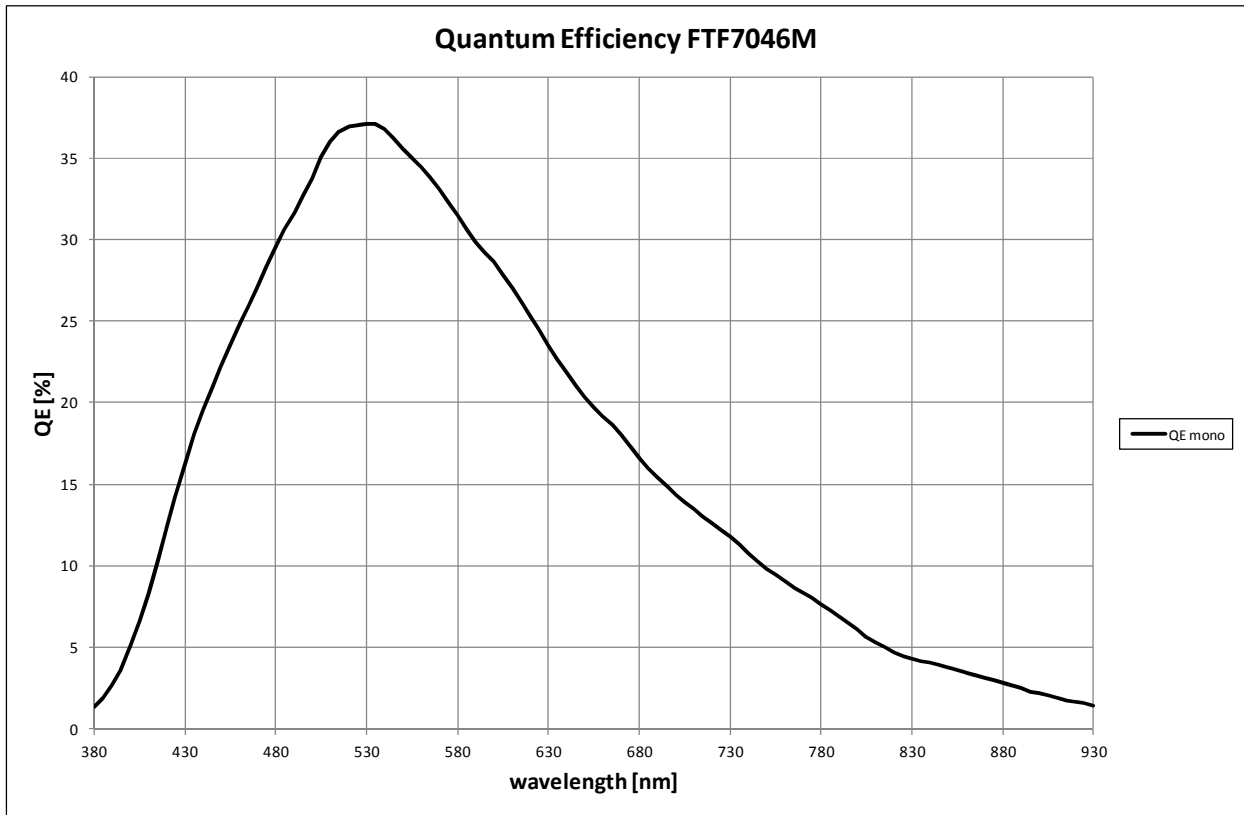


Figure 3: Quantum Efficiency (QE) versus wavelength

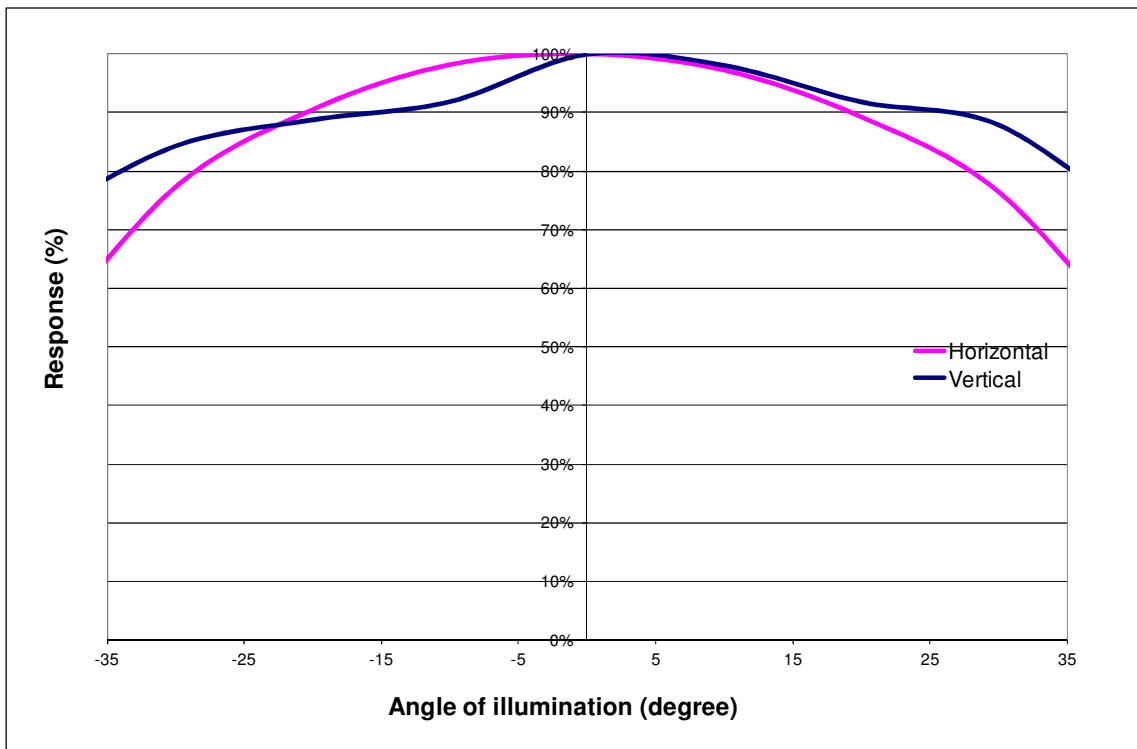


Figure 4: Angular response versus angle of illumination

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DARK CONDITION	MIN	TYPICAL	MAX	UNIT
Dark current level @ 20 °C		5	7	pA/cm ²
Dark current level @ 60 °C	-	130	200	pA/cm ²
Fixed Pattern Noise ¹ (FPN) @ 60°C	-	600	1000	el/s

¹FPN is one-σ value of the high-pass image and normalized at 1 sec integration time

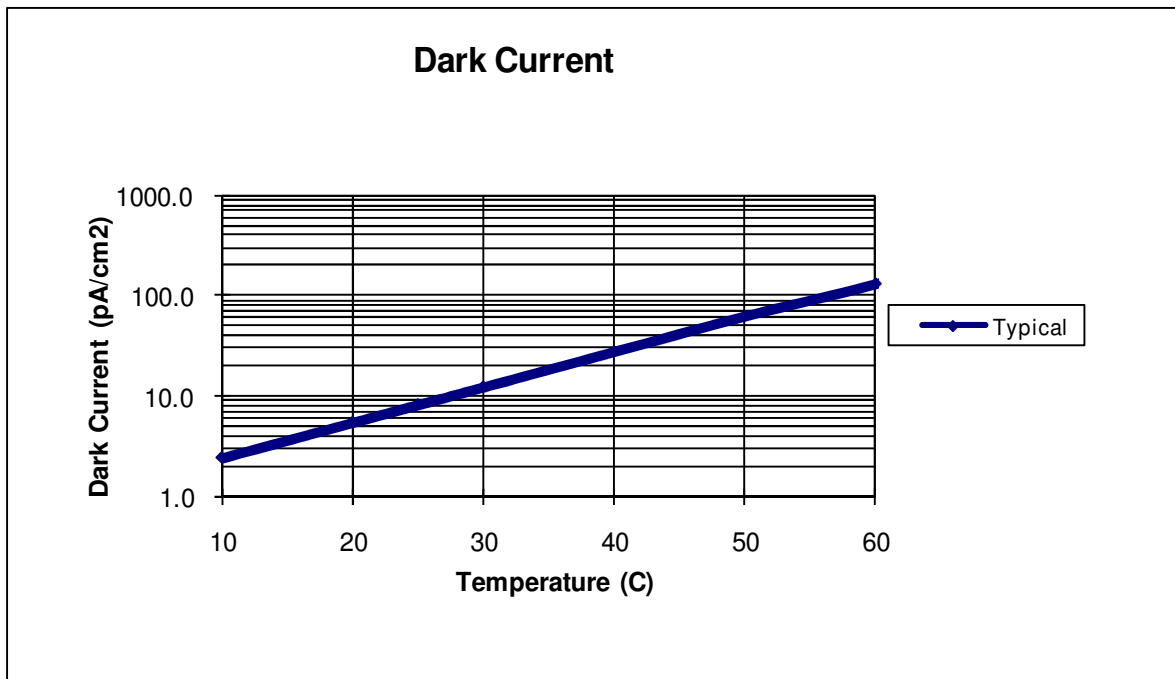
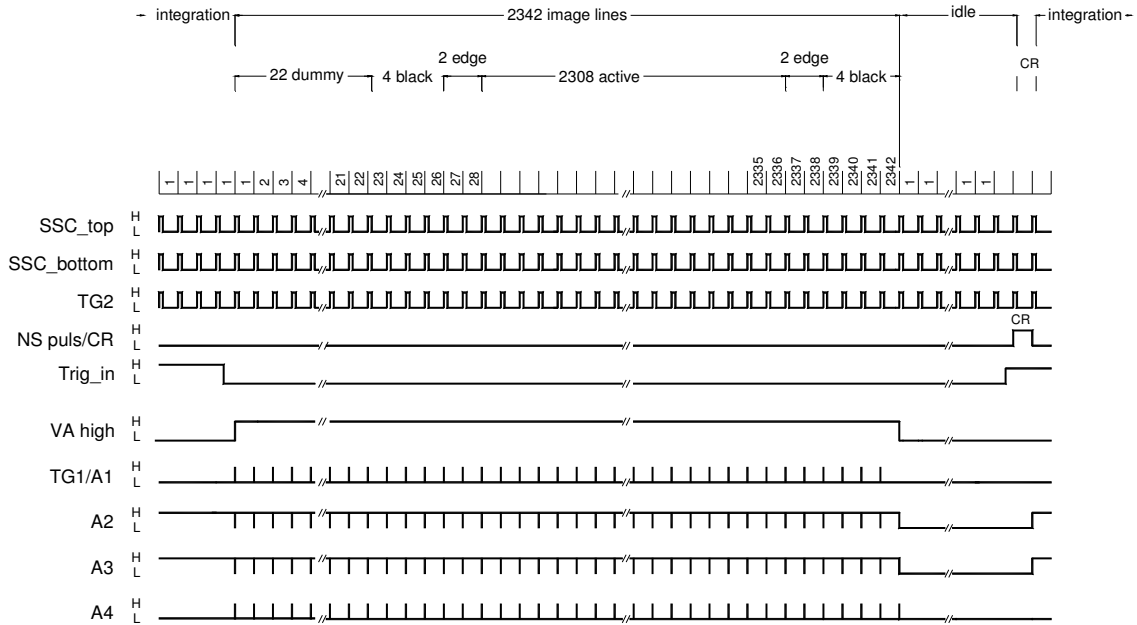


Figure 5: Dark current versus temperature.

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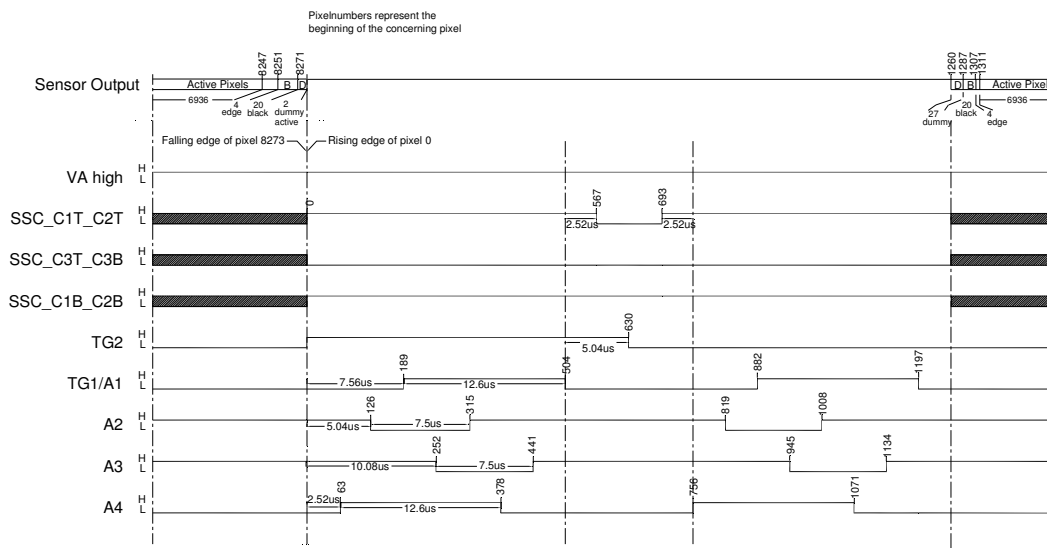
Timing diagrams, standard operation



REMARKS

- * CR is applied during the first line after the transition from L to H of Trig_in
- * CCD is integrating during high period of Trig_in
- * After readout sequence the timing will go into idle mode.

Figure 6: Timing diagram frame transport (dual output)



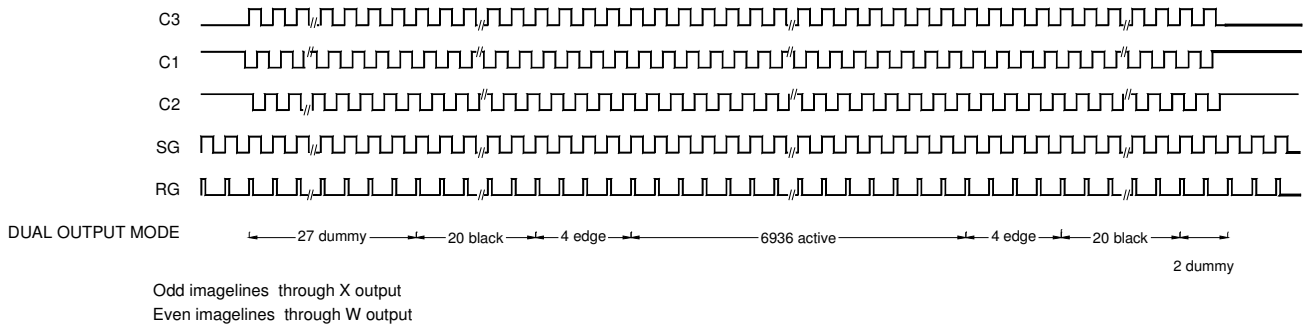
REMARKS

- * Horizontal = 8273 * 1/25E6 = 330.92us
- * Vertical transport frequency = 50kHz

Figure 7: Timing diagram line readout (dual output)

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SENSOR OUTPUT	W			X		
SENSOR PIN	C1T	C2T	C3T	C1B	C2B	C3B
DUAL OUTPUT MODE	C1	C2	C3	C1	C2	C3

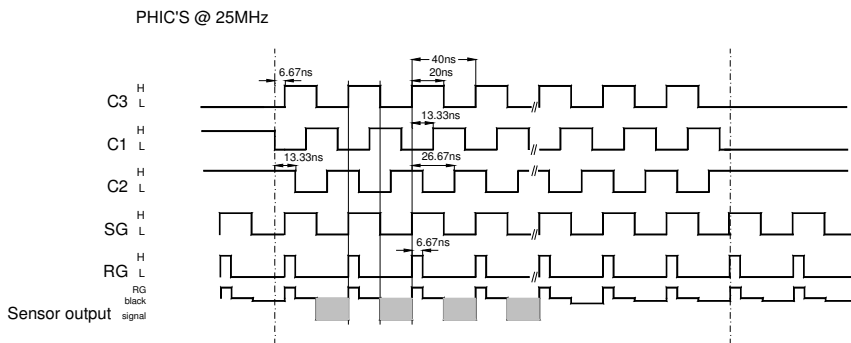


Figure 8: Horizontal readout C-clocks (dual output).

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Application Information

Current handling

One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from overexposure), free electrons are drained to VNS. No current should flow into any VPS connection of the sensor. During high overexposure a total current of 50mA through all VPS connections together may be expected. The npn emitter follower in the circuit diagram (see fig.9) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During high overexposure, a total current of 50mA through all VNS connections together may be expected. The npn emitter follower in the circuit diagram meets these current requirements. The clamp circuit, consisting of the diode and electrolytic capacitor, enable the addition of a Charge Reset (CR) pulse on top of an otherwise stable VNS voltage. To protect the CCD, the current resulting from this pulse should be limited. This can be accomplished by designing a pulse generator with a rather high output impedance.

Decoupling of DC voltages

All DC voltages (not VNS, which has additional CR pulses as described above) should be decoupled with a 100nF decoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. VNS should be decoupled with 1nF decoupling capacitor. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons that build up the charge packets that will reach the floating diffusions only add up to a small current, which will float through VRD. Therefore, a large series resistor in the VRD connection may be used.

Outputs

To limit the on-chip power dissipation, the output buffers are designed with open source outputs. Outputs to be used should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 250 Ω) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is avoided by avoiding a too-small quiescent current in

the emitter follower; about 5mA should do the job. The collector of the emitter follower should be uncoupled properly to suppress the Miller effect from the base-collector capacitance.

A CCD output load resistor of 3.3k Ω typically results in a bandwidth of 130MHz.

Device protection

The output buffers of the FTF7046M are likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera. The RD voltage should always be lower than the SFD voltage.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 10mA. Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-type substrate, we are dealing with some parasitic npn transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram (see fig.9).

Color imaging

The CCD is sensitive from 300nm up to 1100nm. This should be taken into account when using external color filters. The cover glass is not an IR filter.

Unused sections

To reduce power consumption, the following steps can be taken. Connect unused output register pins (C1...C3, SG, OG) and unused SFS pins to zero Volts.

More information

Detailed application information is provided in the application note AN14.

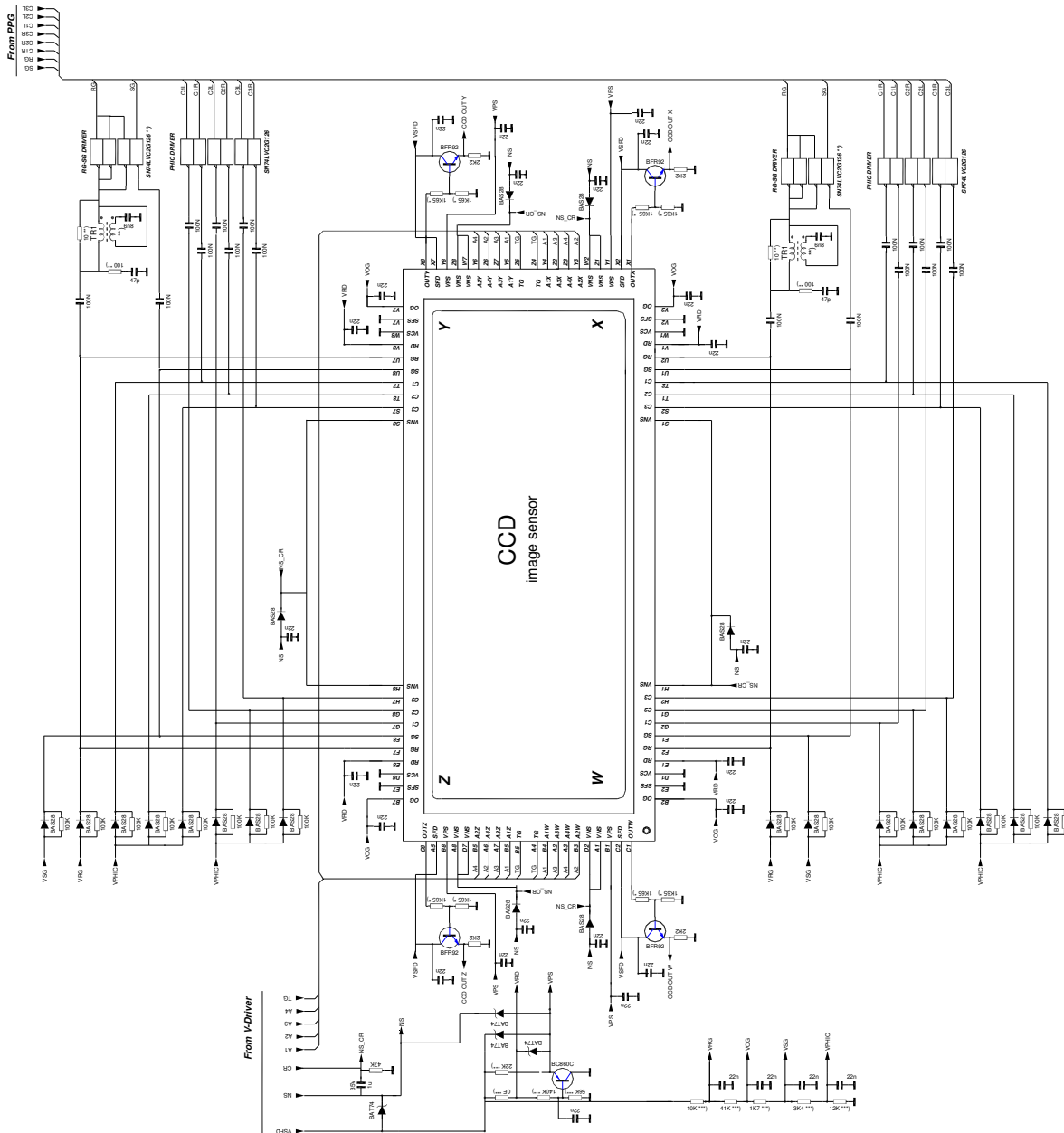


Figure 9: Application diagram

*) Optimal value depends on CDS input range. Total resistor load on sensor output should be 3K3
 **) For 5V RG amplitude use only one buffer and remove TR1 and 100 ohm resistor
 ***) For 10V RG amplitude use 3 buffers in parallel and remove 10 ohm resistor
 ****) Optimal value might be different because of different sensor biasing.
 See datasheet for optimal biasing voltages.

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Device Handling

An image sensor is a MOS device that can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam, and in a dry and dark environment. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in the CCD image sensor process is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remain undamaged. When handling the sensor, use finger cots.

When cleaning the glass we recommend using ethanol. Use of other liquids is strongly discouraged:

- if the cleaning liquid evaporates too quickly, rubbing is likely to cause ESD damage.
- the cover glass and its coating can be damaged by other liquids.

Rub the window carefully and slowly.

Dry rubbing of the window may cause electro-static charges or scratches that can destroy the device.

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Package information

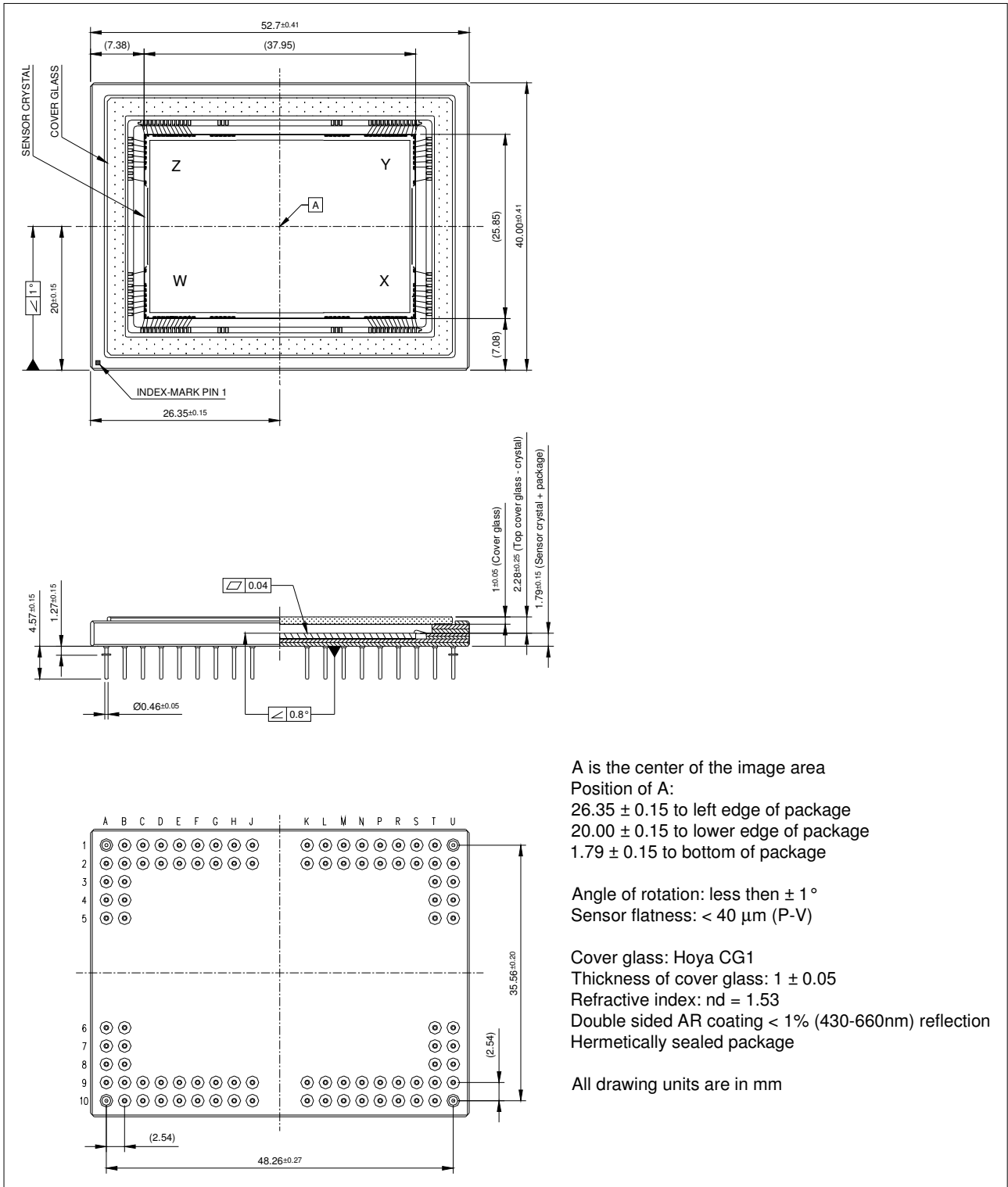


Figure 10: Mechanical drawing of the FTF7046 in PGA Package

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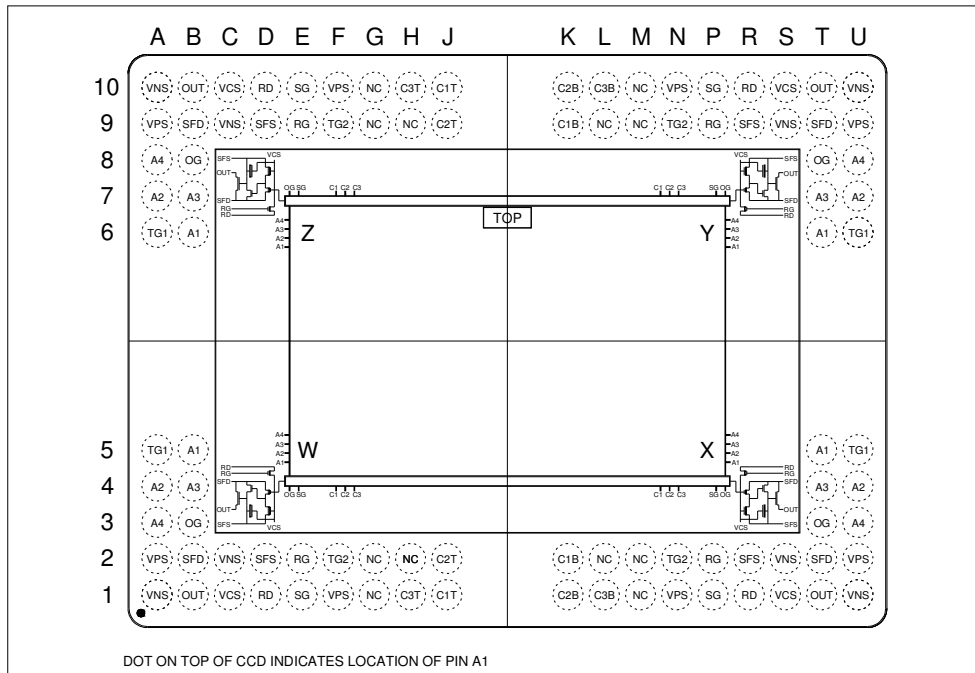


Figure 11: Top view of package showing pin configuration.

SYMBOL	FUNCTION	PIN # W	PIN # X	PIN # Y	PIN # Z
VNS	n-substrate	A1	U1	U10	A10
VNS	n-substrate	C2	S2	S9	C9
VPS	p-well	A2	U2	U9	A9
VPS	p-well	F1	N1	N10	F10
SFD	Source Follower Drain	B2	T2	T9	B9
SFS	Source Follower Source	D2	R2	R9	D9
VCS	Current Source	C1	S1	S10	C10
A1	Image Clock (Phase 1)	B5	T5	T6	B6
A2	Image Clock (Phase 3)	A4	U4	U7	A7
A3	Image Clock (Phase 4)	B4	T4	T7	B7
A4	Image Clock (Phase 2)	A3	U3	U8	A8
TG1	Transfer Gate Image	A5	U5	U6	A6
C1T	Top Register Clock (Phase 1)	J1			J10
C2T	Top Register Clock (Phase 2)	J2			J9
C3T	Top Register Clock (Phase 3)	H1			H10
TG2	Transfer Gate Register	F2	N2	N9	F9
C1B	Bottom Register Clock (Phase 1)		K2	K9	
C2B	Bottom Register Clock (Phase 2)		K1	K10	
C3B	Bottom Register Clock (Phase 3)		L1	L10	
SG	Summing Gate	E1	P1	P10	E10
OG	Output Gate	B3	T3	T8	B8
RD	Reset Drain	D1	R1	R10	D10
RG	Reset Gate	E2	P2	P9	E9
OUT	Output	B1	T1	T10	B10
NC	Not connected	G1	M1	M10	G10
NC	Not connected	G2	M2	M9	G9
NC	Not connected	H2	L2	L9	H9

Table 1: Pinning list

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Order codes

The sensor can be ordered using the following code:

FTF7046M sensor		
Description	Quality Grade	Order Code
FTF7046M/HG	High Grade	9922-157-72111
FTF7046M/IG	Industrial Grade	9922-157-72121
FTF7046M/TG	Test Grade	9922-157-72131
FTF7046M/EG	Economy Grade	9922-157-72151
FTF7046M/CG	Customer Grade	9922-157-72161

**Defect Specifications**

The CCD image sensor can be ordered in a specific quality grade. The grading is defined with the maximum amount of pixel defects, column defects, row defects and cluster defects, in both illuminated and non-illuminated conditions. For detailed grading information, please contact your local Teledyne DALSA representative.

For More Information

For more detailed information on this and other products, contact your local rep or visit our Web site at <http://www.teledynedalsa.com/imaging/products/sensors/>

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