Sapera Vision Software

Sapera™ APF

A Graphical FPGA Development Environment

Key Features

Intuitive Graphical Programming

- Enables Real-time embedded image processing
- Rapid design implementation using Point & Click IDE
- Software centric approach
- Extensive set of image processing functions for the FPGA
- Bit accurate software functions permit verification of algorithm behavior
- Automatic software interface generation for user created hardware designs
- Seamless interface to Xilinx tools

FPGA based Embedded Image Processing Libraries

- Over 150 imaging functions
- Include bit accurate software implementation

Acquisition

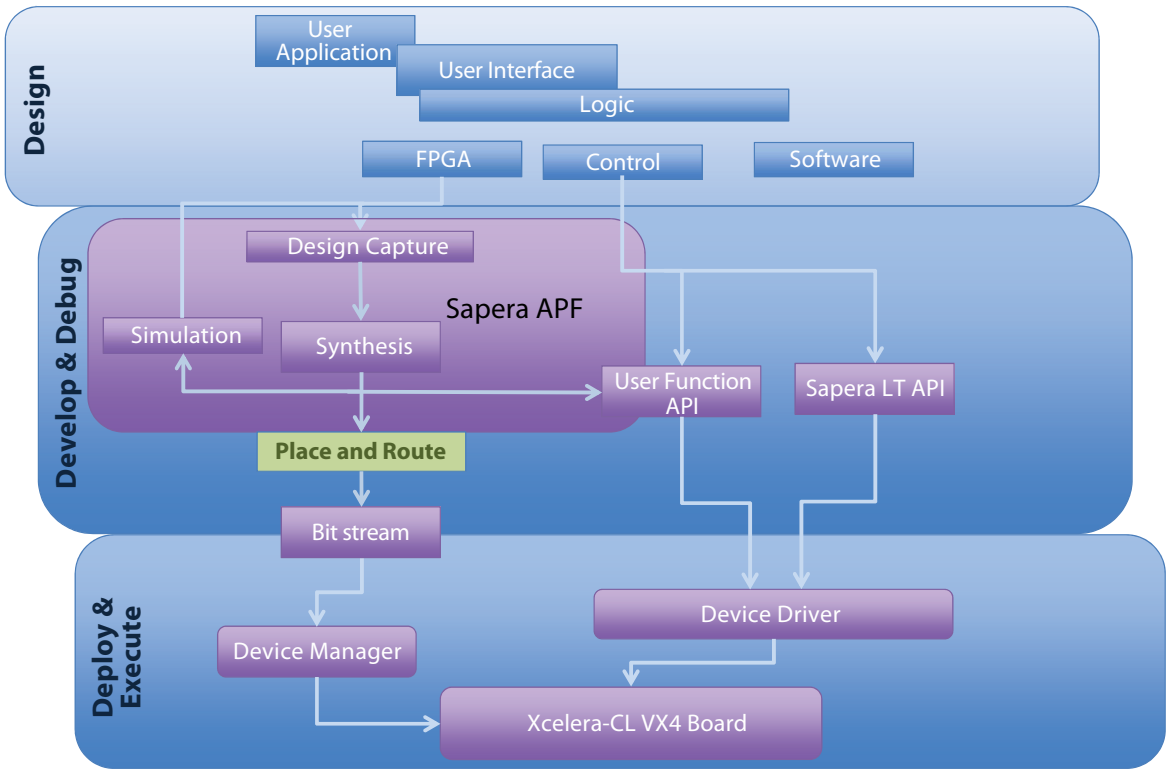
- Capture image from area or line scan cameras
- Color or monochrome processing

TELEDYNE DALSA
A Teledyne Technologies Company

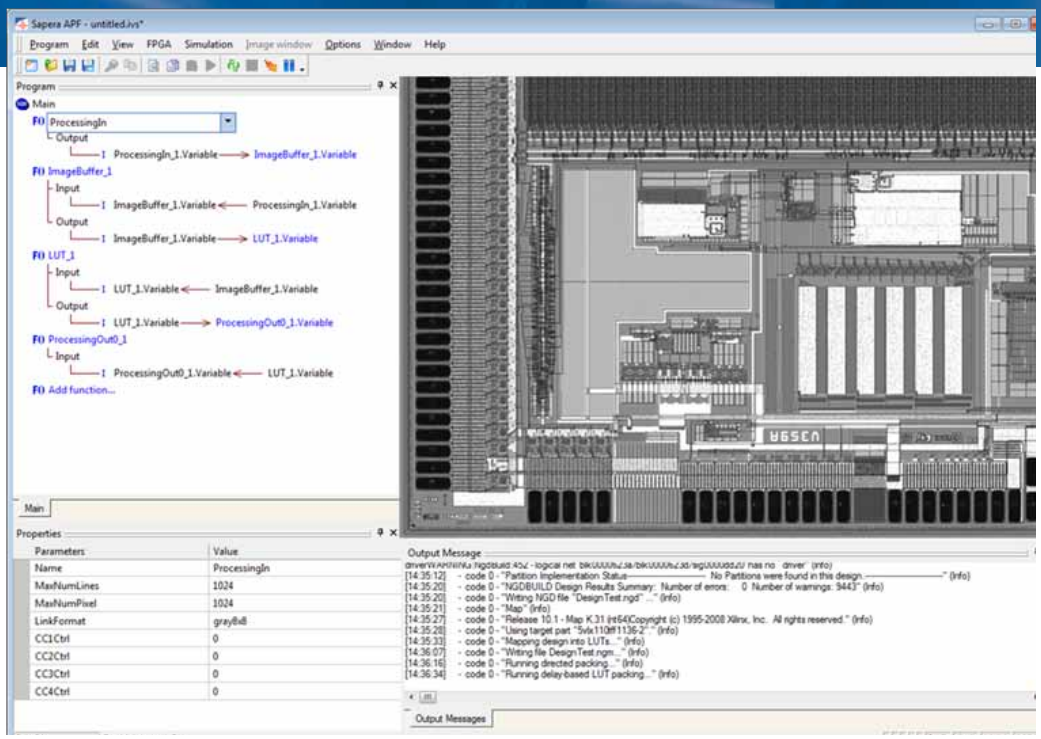
Sapera APF is designed for real-time imaging applications as such it not only offers extensive FPGA image processing functions but also includes libraries for image acquisition, control and auxiliary input/output controls.

Sapera APF's graphical user interface offers programming features of conventional software IDEs like on the fly program editing, single stepping, variable watches to review intermediate results, etc. and combines them with hardware design rules check and resource verification. Users interact with Xilinx tools directly from within Sapera APF to generate FPGA bit streams.

When creating custom FPGA designs, for proper software control, it is necessary to plan and implement equivalent software control functions which includes describing function prototypes and parameters. Sapera APF automates this crucial step of generating software interface for user defined FPGA designs. The user FPGA designs can thus be controlled from Sapera LT based host applications. Sapera APF also comes bundled with RTPro application allowing users to exercise their FPGA designs without having to write control application on the host.



Designing with Sapera APF – An overview



FPGA processing functions

Basic Operations

Arithmetic operations
Logic operations
Pixel operations
Neighborhood operations
Statistics
Camera I/O control
Color Space Conversion
Bayer conversion
Streams
Memory access
GPI/O control

[1] *Contact Teledyne DALSA Sales for availability*

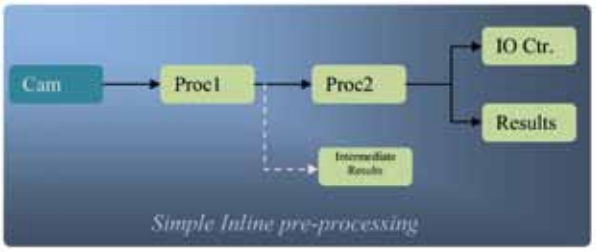
Advanced Operations

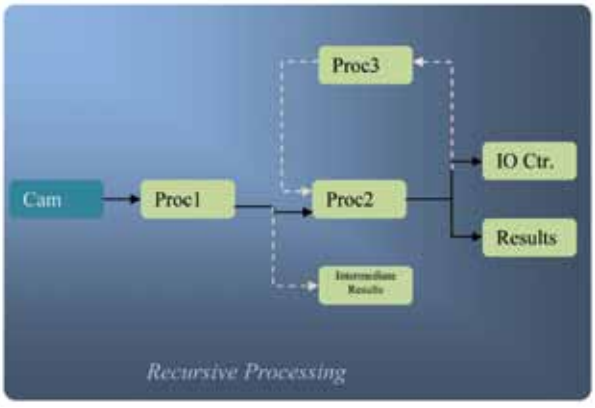
Rotation by arbitrary angle
Loss-less compression
RLE
Image compression

Upcoming Functions[1]

Warping
Wavelet Encoding
Blob Analysis
JPEG Compression

Processing Topologies





Development Requirements:
Microsoft Windows XP, Windows 7 32/64-bit
Intel Core2 Duo class CPU
2GB of RAM
1GB of Hard drive space
Xilinx ISE 10.1 or higher
Microsoft Visual Studio 2005 or higher (for software control projects)

Deployment Requirements:
Teledyne DALSA Xcelera-CL VX Series vision processors
Microsoft Windows XP, Windows 7 32/64-bit

www.teledynedalsa.com

Americas
Boston, USA
+1 978-670-2000
sales.americas@teledynedalsa.com

Europe
Munich, Germany
+49 8142-46770
sales.europe@teledynedalsa.com

Asia Pacific
Tokyo, Japan
+81 3-5960-6353
sales.asia@teledynedalsa.com

Shanghai, China
+86 21-3368-0027
sales.asia@teledynedalsa.com

Teledyne DALSA is an international leader in digital imaging and semiconductors and has its corporate offices in Waterloo, Ontario, Canada.

TELEDYNE DALSA
A Teledyne Technologies Company