Rad-icon Imaging Corp

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AN11: Analog Readout Circuitry for RadEye™ Sensors

Introduction

Rad-icon Imaging Corp. offers its RadEye sensor modules in two ways: either bundled with a fully functional camera board and imaging software, or as a bare module with no readout circuitry or software. In the second case, the customer will have to provide his or her own readout circuitry. This application note suggests a design for the analog portion of the readout circuitry which will cover the pinout of the RadEye sensor, the amplification of the RadEye's differential output, and some basic timing considerations for use in conjunction with an AD9221 analog to digital converter (ADC). For complete information on the AD9221 please refer to the data sheets on the Analog Devices website at http://www.analog.com/.

RadEye™ Pinout

The RadEye sensor uses the Samtec FC1-15-01 connector to connect to the supply voltage, clocks, ground, and reference voltage necessary for operation (Figure 1). One input signal of note is the signal denoted on Figure 1 as VD. VD is a reference voltage for the digital readout circuitry within the RadEye sensor. For optimal sensor performance the signal should remain constant at 3.8±0.2V. The RadEye does not draw a substantial amount of current from this source, so a simple voltage divider will be sufficient. The START and CLOCK inputs, and the FRAME and LINE outputs, are part of the timing circuitry and are addressed in the RadEye1 and RadEye100 data sheets. OUTS and OUTR represent the differential analog output of the sensor.

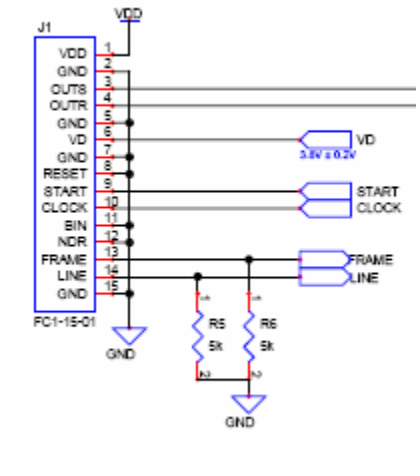


Figure 1
Sensor Pinout

Amplification of the Differential Output

The most important and challenging component of the analog readout design is the amplification of the RadEye's differential output. A typical differential amplifier design is shown in Figure 2. A suitable Op-Amp is also suggested.

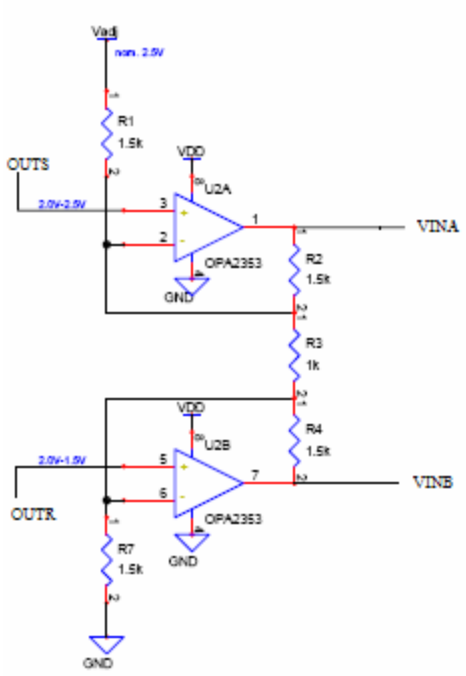


Figure 2
Differential Amplifier

The circuit is analyzed as follows:

For simplicity OUTS, OUTR, V_{adj}, VINA and VINB will be referred to as VS, VR, VAD, VA and VB, respectively. R1, R2, R4, and R7 will be referred to as R, and R3 will be referred to as RG.

1. Apply Kirchhoff's Current Law to the node where R2 meets R3.

Eq1:

$$\frac{(VS - VR)}{RG} = \frac{(VA - VS)}{R} + \frac{(VAD - VS)}{R}$$

2. Solve for VA.

Eq2:

$$VA = \frac{(R + 2 * RG)}{RG} * VS - \frac{R}{RG} * VR - VAD$$

3. Apply Kirchhoff's Current Law to the node where R3 meets R4.

Eq3:

$$\frac{(VS-VR)}{RG}=\frac{VR}{R}+\frac{(VR-VB)}{R}$$

4. Solve for –VB

Eq4:

$$-VB=\frac{R}{RG}*VS-\frac{(R+2*RG)}{RG}*VR$$

5. Combine Equation 2 and Equation 4.

Eq5:

$$VA-VB=2*\frac{(R+RG)}{RG}*(VS-VR)-VAD$$

Therefore, the differential output has been given a gain of 2*(R+RG)/RG and an offset of -VAD. Rad-icon suggests a gain of 5 with an offset of 2.5 for most applications. This keeps VA and VB safely within the rails of the shown Op-Amps (Figure 2) and ADC (Figure 3) and sets the minimum and maximum difference voltages to -2.5V and 2.5V respectively upon arrival at the ADC (-2.5V to 2.5V is the FSR of the AD9221 shown in Figure 3).

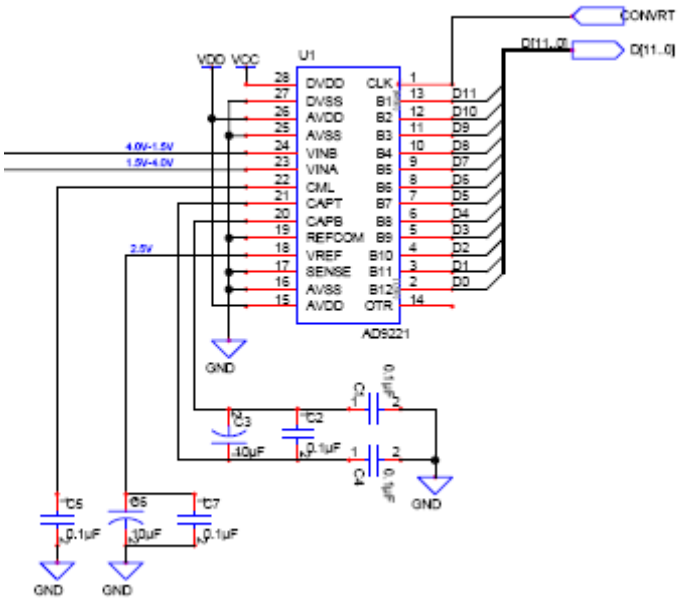


Figure 3
AD9221 Circuit

It is important to note two things about VAD. First, VAD is not scaled by the gain factor, so it can be freely adjusted independent of the amplifier gain. This allows for easy adjustment of the zero signal level. To ensure that no pixels generate values below the ADC zero level, the suggested range for the zero signal level is between 50-100 LSB. Second, VAD must supply current to the amplifier circuit. Therefore, a low-impedance source such as an op-amp or a voltage regulator should be used to generate VAD.

Another important consideration for the differential amplifier circuit is that resistors R1, R2, R4, and R7 should be kept at the same value for the aforementioned transfer characteristic to hold.

Plots

Figure 6 (on page 6) shows three plots that demonstrate different aspects of equation 5. The plot in the upper left shows the sensitivity of the camera in µV/LSB and the maximum voltage swing allowable on VS and VR before the camera saturates. This shows that there is a tradeoff between sensitivity and dynamic range. If the gain is set very high, the camera will respond to very small fluctuations in VS and VR; however, the camera will saturate with a smaller deviation from the zero level of two volts on VS and VR. The plot in the upper right essentially shows the same thing as the aforementioned plot by plotting VA and VB against VS for various different gain settings. With increasing gain, the slopes of VA and VB become steeper. This indicates a higher level of sensitivity. However, the plot also demonstrates that the steeper slopes lead to a faster approach of the rails (0V and 5V), therefore saturating more quickly. The final plot (bottom) shows a plot of camera gain versus gain resistor value. This assumes that the value of R is fixed at 1.5kΩ. Note that the gain is not linear with respect to the gain resistor value.

Timing

Figure 4 shows the timing diagram for the RadEye sensors. Detailed timing explanations can be found in the RadEye1 and RadEye100 data sheets. For the analog board design it is only necessary to comment on appropriate sampling on the ADC. As can be seen from the diagram the OUTS and OUTR signals are produced during the low half of the master clock cycle. Due to the slight skew provided by the circuitry within the RadEye sensor itself, a good time to sample (drive the CONVRT signal on the ADC high) is on the rising edge of the master clock. Sampling on the rising edge of the master clock gives the output voltages the maximum possible time to stabilize.

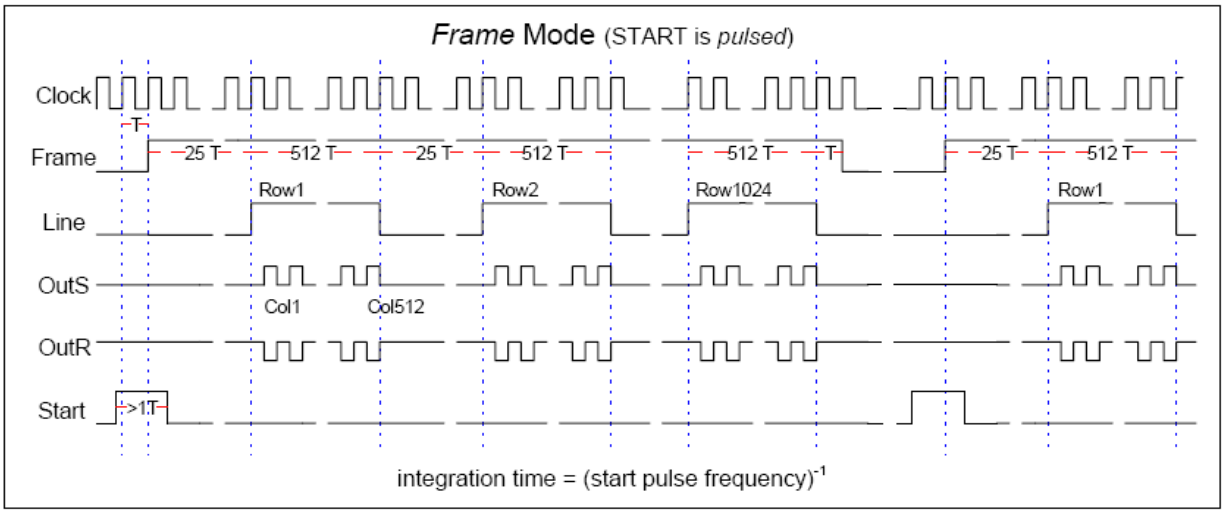


Figure 4
Timing Diagram

Conclusion

A simple differential amplifier circuit and a basic understanding of the timing of the RadEye sensor are required to create a circuit that will allow an AD9221 ADC to digitize the image information from the RadEye sensor. Please refer to the AD9221 data sheet for additional application information, as it is a very complicated IC. This circuit is intended for reading out frames in the RadEye's standard readout mode (i.e. BIN, SCAN and NDR are all held low). The design can be duplicated for RadEye modules consisting of more than one sensor. The full schematic can be found on the next page (Figure 5).

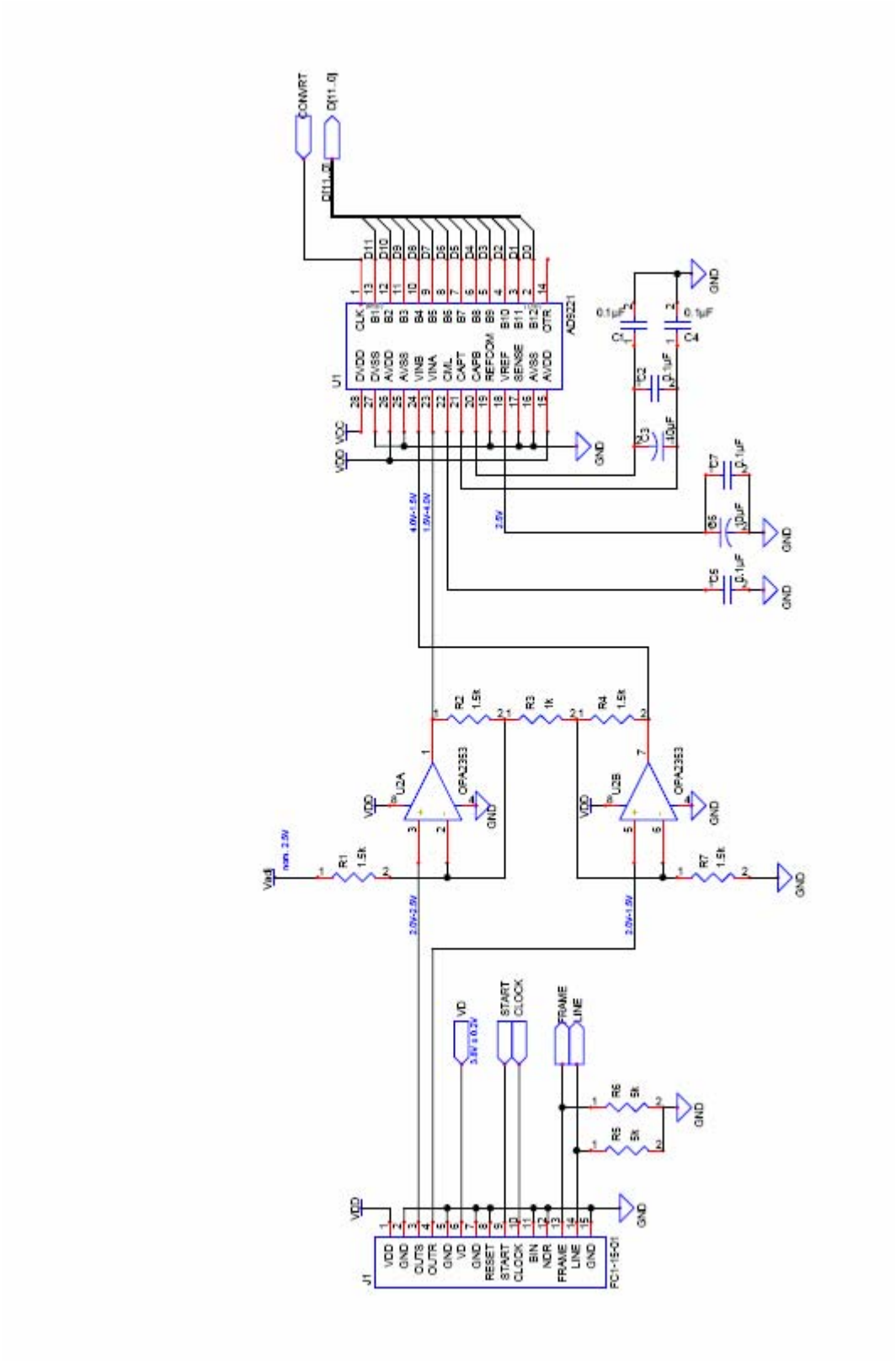
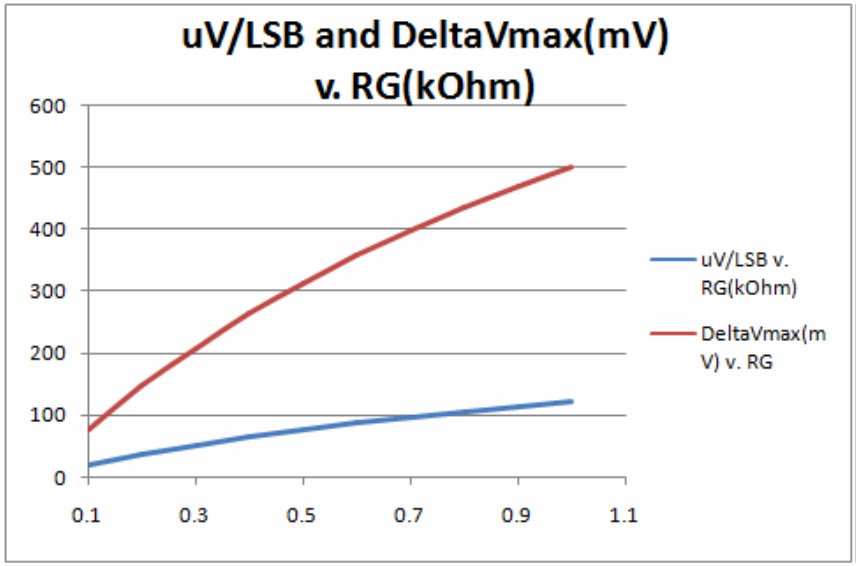
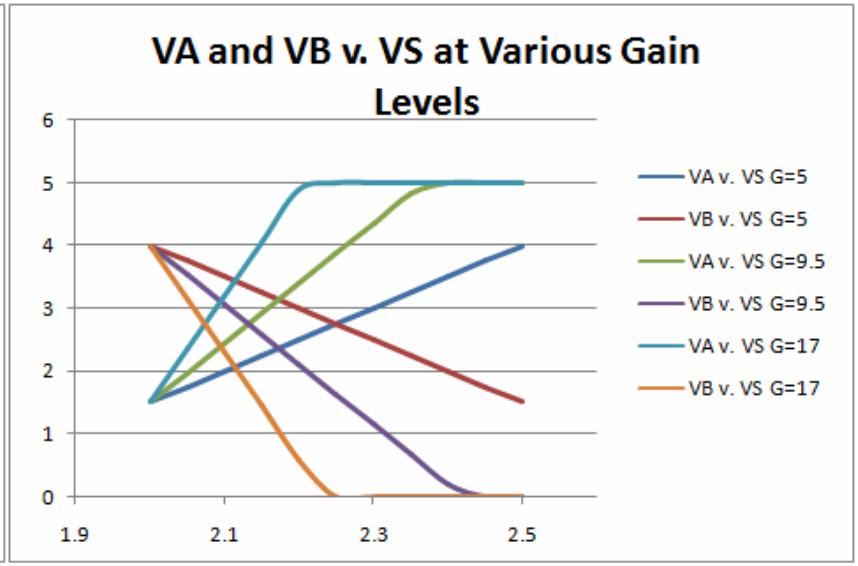


Figure 5
Full Schematic





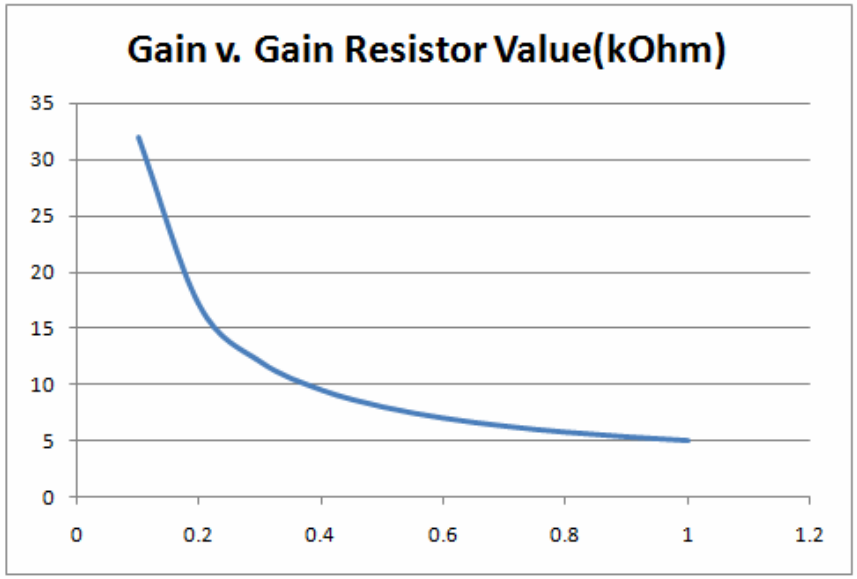


Figure 6
Plots